A New Multipulse Technique for Probing Electron Trap Energy Distribution in High-κ Materials for Flash Memory Application

Xue Feng Zheng, Wei Dong Zhang, Bogdan Govoreanu, *Member, IEEE*, Jian Fu Zhang, and Jan van Houdt, *Senior Member, IEEE*

***Abstract*—A new discharge-based multipulse technique has been developed in this paper, which overcomes the shortcomings of the existing techniques, such as the charge pumping, charge injection and sensing, and two-pulse C–V techniques. It captures the energy signature for electron traps across high-κ materials and can be a useful tool for material selection during technology development. Trap distributions in HfO_2, Al_2O_3, and HfAlO have been compared to identify the effects of material variation. It is observed that hafnium gives the shallow traps at about 0.45 eV above the silicon conduction band bottom (Si E_{CB}), and the deep traps at 0.8 eV below the Si E_{CB} are caused by aluminum. HfAlO combines the features in HfO_2 and Al_2O_3. A peak near the Si E_{CB} has been observed in all the three materials.**

***Index Terms*—Electron trap, energy distribution, Flash memory, floating gate, high-κ dielectrics, interpoly dielectric (IPD), pulsed I–V.**

I. Introduction

The APPLICATION of high-κ materials, such as Al_2O_3 or HfAlO, is essential for downscaling the Flash memory technology beyond the 30-nm generation in order to reduce the leakage current through the dielectric layers [1]–[3]. For floating-gate Flash cells, planarization is inevitable for further downscaling, which will result in the loss of the sidewall overlapping on the floating gate and will lead to a significant reduction of the coupling ratio. An interpoly dielectric (IPD) stack with higher dielectric constant will increase the capacitance without reducing its physical thickness and therefore help in maintaining the coupling ratio [1]. In charge-trapping Flash cells, such as TANOS $(TaN(TiN)/Al_2O_3/Si_3N_4/SiO_2/Si)$, Al_2O_3 was proposed to replace SiO_2 as the blocking dielectric layer, since its higher dielectric constant will ensure a larger physical thickness at the same EOT and will suppress the leakage current [4].

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X. F. Zheng was with the School of Engineering, Liverpool John Moores University, L3 3AF Liverpool, U.K. He is now with the School of Microelectronics, Xidian University, Xi'an 710071, China.

W. D. Zhang and J. F. Zhang are with the School of Engineering, Liverpool John Moores University, L3 3AF Liverpool, U.K. (e-mail: W.Zhang@ljmu.ac.uk).

B. Govoreanu and J. van Houdt are with the TU/PT Division, Interuniversity Microelectronics Center, 3001 Leuven, Belgium.

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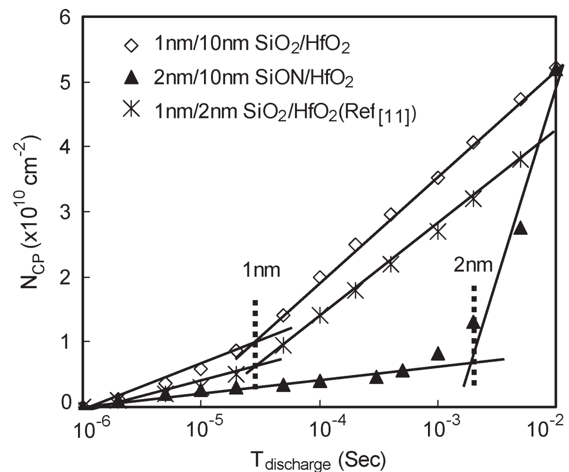

Fig. 1. CP results on SiO_2/HfO_2 stacks with different SiO_2 thickness (stacks 1 and 4). The sharp increase in the slope at the dotted line is caused by transition from SiO_2 to HfO_2. Test conditions are $V_{\rm charge} = 1.5$ V, $V_{\rm base} = -1.5$–0.5 V, $t_{\rm rf} = 0.3$ μs, and $t_{\rm charge} = 100$ μs.

The progress of using high-κ materials for nonvolatile memory has been held back by the large defect density in high-κ materials, which is a few orders of magnitude higher than that in conventional SiO_2 [5]–[7]. This limits the memory retention due to the excessive low-field leakage current induced by trap-assisted tunneling [8]. For accurate retention prediction and fast material and processing optimization, characterization of the low-field leakage current is required. In Flash memory cells, this current is too small to be detected directly by electrical measurements. Theoretical modeling is therefore required to estimate the low-field leakage current. Electron trap energy distribution in the bulk of high-κ materials is the essential information required for accurate modeling [8], [9]. However, the detailed information on the overall distribution is still largely missing.

Various charge-pumping (CP) techniques have recently been used to characterize the energy/spatial distribution of electron traps in high-κ materials [10]–[12]. However, CP can only reach the traps at around 2 nm from the substrate interface [13], since its maximum discharge time is limited practically at 10 ms. This can be clearly seen in Fig. 1, in which the results obtained by the CP technique with variable discharge times on SiO_2/HfO_2 stacks with different SiO_2 thickness are shown. The sharp increase in the slope at the dotted line is caused by the transition from SiO_2 to HfO_2, indicating that the trap density in

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the SiO_2 interfacial layer is much smaller than that in the high-κ bulk and can be safely neglected. Most traps in thick high-κ films required for Flash application cannot be probed by CP. Moreover, CP techniques with variable discharge bias can only probe traps at energy levels corresponding to the Si bandgap [12]. No information on trapping at energy levels outside the Si bandgap can be obtained.

A new technique, charge injection and sensing (CIS), was developed to probe trap distribution at the electron injection level through sweeping the injection bias [14]. However, only a limited region above the Si E_{CB} within 2–3 nm into the high-κ bulk can be probed by the CIS technique for a 1-nm/12-nm SiO_2/Al_2O_3 stack when the maximum charging time is 2000 s. Majority traps in the bulk cannot be probed. The traditional $C-V/I-V$ techniques have been used to probe charge loss at long time scales [15], [16], and photo I–V technique was used to assess the spatial distribution of charges [17], but these measurements are too slow to characterize the defects near the interface because of fast detrapping [6], [7]. The single-pulse I–V technique was developed to overcome the fast detrapping, but it did not give the energy and spatial distribution of defects [18]. We have recently developed a two-pulse C–V measurement technique that can overcome the shortcomings of conventional techniques and probe the electron traps throughout the SiO_2/high-κ stack [19], [20]. It was shown that electron traps in the bulk of high-κ layer indeed dominate the trapping, and the electron trap energy distribution below Si E_{CB} throughout the SiO_2/Al_2O_3 stack can be obtained. However, the two-pulse C–V technique cannot probe the trap distribution above Si E_{CB} in the high-κ bulk, as explained in Section III-A.

A new discharge-based multipulse (DMP) technique is developed in this paper, which gives the electron trap energy distribution both above and below Si E_{CB} throughout the SiO_2/high-κ stack. Limitations in techniques such as CP, CIS, and two-pulse C–V have been overcome. Trap distributions in HfO_2, Al_2O_3, and HfAlO have been extracted and compared to identify the effects of material variation on the distribution. This paper is organized as follows. After a description of the devices and measurement setup in Section II, the methodology used to develop the DMP technique and the detailed procedure are given in Section III-A. Energy distributions of electron traps across the dielectric stacks with Al_2O_3, HfO_2, and HfAlO layers are extracted and compared in Section III-B.

II. Devices and Experiments

A summary of the samples used in this paper is given in Table I. Poly-gate nMOSFETs with SiO_2/high-κ gate dielectric stacks were fabricated at IMEC. Either a 1-nm IMEC-clean SiO_2 or a 2-nm SiON was deposited as the bottom layer. A 10-nm or 12-nm high-κ layer was then prepared by atomic layer chemical vapor deposition using a process flow similar to that used for forming the IPD stacks in floating-gate Flash memory devices. The deposition was followed by a conventional postdeposition anneal for stacks 1, 2, and 4. Rapid thermal annealing at 900 °C was carried out on all samples for 30 s after the n+ poly deposition. The sample-to-sample variation is negligible.

TABLE I
Summary of the Samples Used in This Paper

Stack	Process condition summary
1	1 nm SiO_2 /10 nm ALD HfO_2 with PDA@550 °C in N_2, poly gate.
2	2 nm SiON /10 nm ALD Al_2O_3 with PDA@700 °C in N_2, poly gate.
3	2 nm SiON /12 nm ALD HfAlO without PDA, poly gate.
4	2 nm SiON /10 nm ALD HfO_2 with PDA@500 °C in O_2, poly gate.

RTA at 900 °C was carried out for 30 s after the n+ poly deposition. All devices are nMOSFETs.

The pulsed I–V technique [6], [18] is used to measure the threshold voltage of the device under test. The measurement system consists of an Agilent 81101A pulse generator, a current–voltage converter, and an Agilent DSO6104 oscilloscope. The shift of threshold voltage ΔV_{th} induced by electron trapping/detrapping is measured at a constant drain current of 1×10^{-4} A with a drain bias at 100 mV. It is then converted to an equivalent trap sheet density at the substrate interface [16].

III. Results and Discussions

A. DMP Technique

There are two shortcomings for the two-pulse C–V technique [20]. First, it does not allow probing traps with energy level above the silicon conduction band bottom E_{CB}, since the gate bias applied during discharge $V_{\mathrm{discharge}}$ must be lower than the flatband voltage V_{FB} [19]. Second, after each discharging time, the device was stressed again to refill the traps. To obtain a trap distribution, many time points are needed, and the repeated stress can damage the device.

The DMP technique is designed to overcome the shortcomings mentioned earlier. Fig. 2(a) shows that the device is only filled once here. The gate bias is then lowered to $V_{\mathrm{discharge1}}$ for discharging. Unlike the two-pulse C–V, $V_{\mathrm{discharge1}}$ here can be higher than V_{FB}, since the discharging is monitored from the I_d–V_g shift obtained by applying reversed short pulses (5 μs) [21] at various intervals during discharging. Once the discharging reaches saturation, V_g is lowered to $V_{\mathrm{discharge2}}$, and the process is repeated until the discharge bias becomes smaller than V_{th}, and from there onward, the direction of the short pulses is changed so that V_{th} can be measured, as shown in Fig. 2(b).

Under a given $V_{\mathrm{discharge}}$, only electron traps with energy level higher than the silicon conduction band bottom can be discharged via tunneling [13], since there are little empty states in the silicon bandgap. If a gate bias gives the corresponding potential drop of V_{SiO2} across the SiO_2 layer, the energy level of electron traps will change by $\Delta E_{\mathrm{IL}} = qV_{\mathrm{SiO2}}$ in the high-κ layer at the SiO_2/high-κ interface and by $\Delta E_G = qV_{\mathrm{dielectric}}$ at the gate interface, as shown in Fig. 2(c). The traps within the energy range of ΔE_{IL} and ΔE_G become dischargeable. The energy spectroscopy of electron traps can therefore be measured by sweeping the gate bias, and ΔE_{IL} can be used as an indicator for the energy range [19], [20].

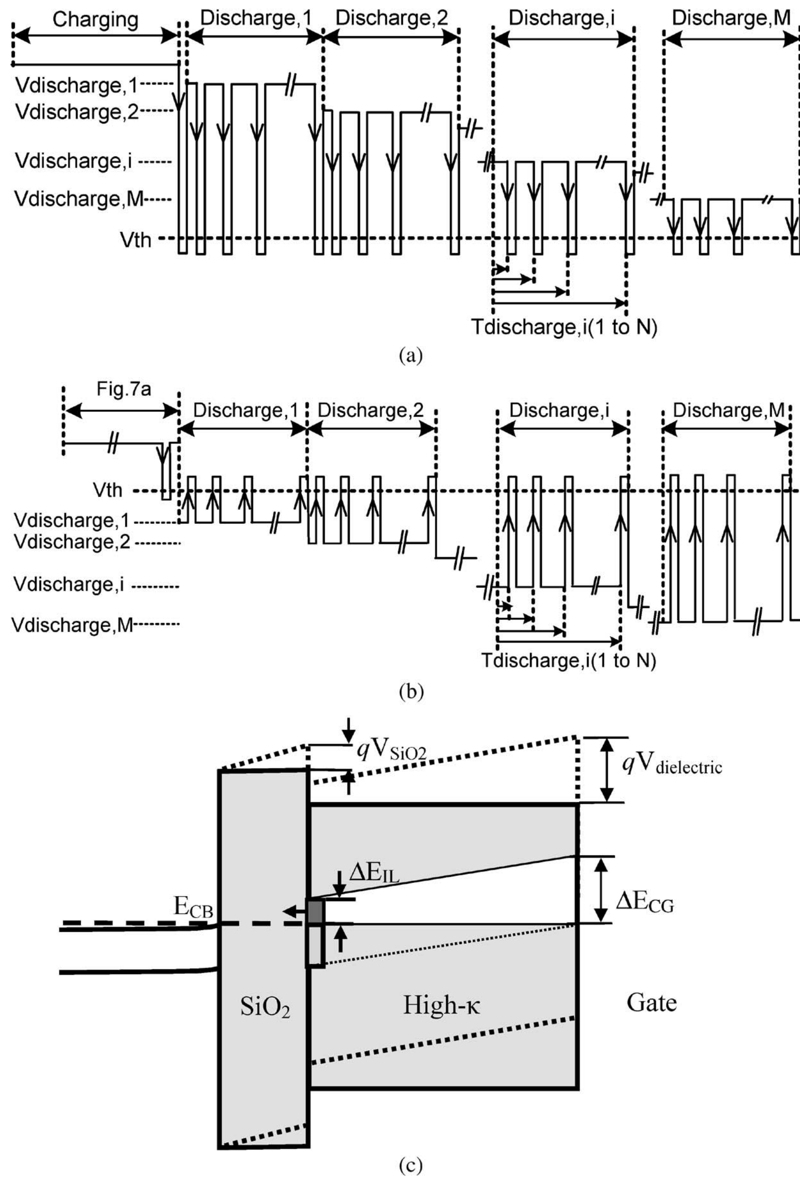


Fig. 2. (a) Illustration of the waveform for the DMP technique when $V_{\mathrm{discharge}} > V_{\mathrm{th}}$. After charging, a number of lower voltages ($V_{\mathrm{discharge},1} \sim V_{\mathrm{discharge},m}$) are sequentially applied to discharge shallow traps. For each $V_{\mathrm{discharge}}$, a new saturated trapping level is observed, and the discharge is interrupted by short pulses of 5-μs edge time to measure V_{th}. (b) Illustration of waveform for the DMP technique when $V_{\mathrm{discharge}}$ is reduced below V_{th}. The short pulses change direction in order to measure V_{th} from the pulse edge. By combining Fig. 7(a) and (b), the energy distribution both below and above Si E_{CB} can be measured. (c) Energy band diagram of the SiO_2/high-κ stack during discharge at a negative gate bias. If a gate bias gives the corresponding potential drop of V_{SiO2} across the SiO_2 layer, the energy level of electron traps will change by $\Delta E_{\mathrm{IL}} = qV_{\mathrm{SiO2}}$ in the high-κ layer at the SiO_2/high-κ interface and by $\Delta E_G = qV_{\mathrm{dielectric}}$ at the high-κ/gate interface. $V_{\mathrm{dielectric}}$ is the potential drop across the SiO_2/high-κ stack.

Fig. 3 shows the detailed test procedure. Note that, during discharging, electron trapping level changes significantly due to the high trapping density in the high-κ layer. This causes V_{th} to shift accordingly and, in turn, changes the potential drop across the SiO_2 layer. To take this into account, each V_{th} measured at the discharging intervals is used as the monitor of effective trapping level in the dielectric stack, and the discharge bias is adjusted accordingly to ensure that V_{SiO2} and, therefore, ΔE_{IL} at the SiO_2/high-κ interface are kept constant during discharge [20].

We now discuss the trap filling in more details. In order to measure the trapping density through discharging across the high-κ layer, electron traps need to be filled first. By applying a high positive bias on the gate, electrons can be injected into the conduction band of the high-κ layer and fill the traps via scattering. The trap-filling time should be long enough so that saturation in trapping is achieved. The typical I_d–V_g curves measured by the pulsed I–V technique during charging are shown in Fig. 4(a), and the extracted ΔV_{th} shift is shown in Fig. 4(b). It shows that saturation is reached within 100 s for the samples used in this paper. In order to check if the trap filling generates new electron traps, the trapped electrons are completely discharged before a second trap filling is carried out on the same device. Fig. 4(b) shows that there are few new traps generated during the first filling, as good agreement is observed between the first and the second filling.

It is noted that there is also detrapping during the trap-filling step. Detrapping during the trap-filling step mainly occurs near

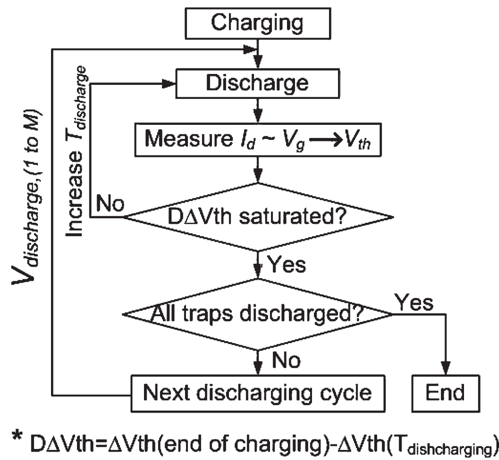


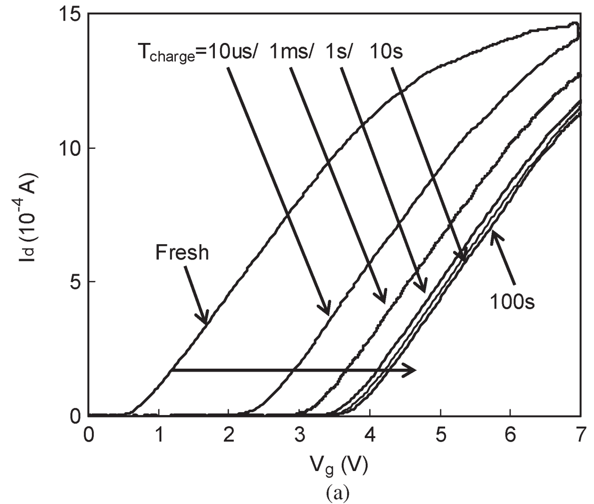
Fig. 3. Flowchart of the test procedure. V_{th} measured at the end of each discharge stage is used as the initial V_{th} of the following discharge stage.

the gate interface and at shallow energy level. The current technique is unable to probe the traps that cannot be filled steadily. It should be pointed out that these unfilled traps will not contribute to ΔV_{TH} for Flash memory. After the trap filling is saturated, the gate bias is reduced to discharge the electron traps. Switching to a lower gate bias will reduce tunneling current and raise the trap energy level against Si E_{CB}. This, in turn, reduces trapping rate and enhances detrapping so that further trap filling in the bulk of dielectric during detrapping must be negligible. It is possible that trap filling near the gate may increase, but the ΔV_{TH} used here is insensitive to it.

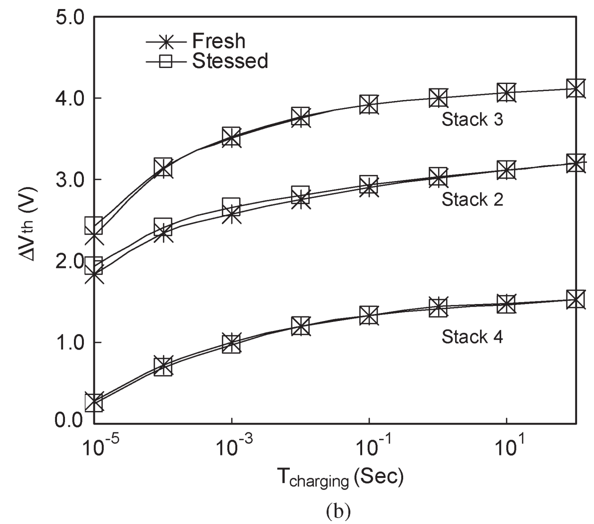
Fig. 5 shows the extracted trapping level at different $T_{\mathrm{discharge}}$ during a discharge at $V_{\mathrm{discharge}} = -5$ V after the trap filling. Their difference, $D\Delta V_{\mathrm{th}} = \Delta V_{\mathrm{th}}$ (end of charging) $-$ ΔV_{th} ($T_{\mathrm{discharge}}$), is the discharge-induced V_{th} shift, which can be converted into the equivalent trap sheet density at the substrate interface, i.e., ΔN_{DMP}. Given a long-enough $T_{\mathrm{discharge}}$ and a large-enough negative bias, all traps throughout the stack can be discharged as $D\Delta V_{\mathrm{th}}$ approaches the trapping level. This confirms that, unlike the CP and CIS techniques, the new DMP technique allows probing traps throughout the stack. The fact that $D\Delta V_{\mathrm{th}}$ saturates at the trap-filling level indicates that additional trap-filling-induced ΔV_{th} during the detrapping phase is negligible.

B. Energy Distribution of Electron Traps

Energy distribution of electron traps across the high-κ layer is obtained by using the DMP technique to measure the discharged trap density against the corresponding ΔE_{IL}. A typical result of discharging under all given $V_{\mathrm{discharge}}$ against $T_{\mathrm{discharge}}$ is shown in Fig. 6(a) for a 2-nm/10-nm SiON/Al_2O_3 stack. The end point for one curve is the starting point for the curve immediately above it. It is clear that detrapping occurs even under a positive bias when its value is reduced, caused by the discharge of shallow traps. The cumulative ΔN_{DMP} measured at the last point of each discharge against the corresponding ΔE_{IL} is shown in Fig. 6(b). Nearly 60% of the traps in Al_2O_3 are below Si E_{CB}, in agreement with the observation by using the two-pulse C–V technique [20]. There is a large



(a)



(b)

Fig. 4. (a) I_d–V_g during charging the 2-nm/10-nm SiON/Al_2O_3 stack (stack 2) measured by a pulsed technique. $V_{\mathrm{charging}} = 7$ V. (b) Trap-charging kinetics on the fresh and the stressed-then-discharged device. Little trap generation is observed for the SiON/high-κ stacks used in this paper.

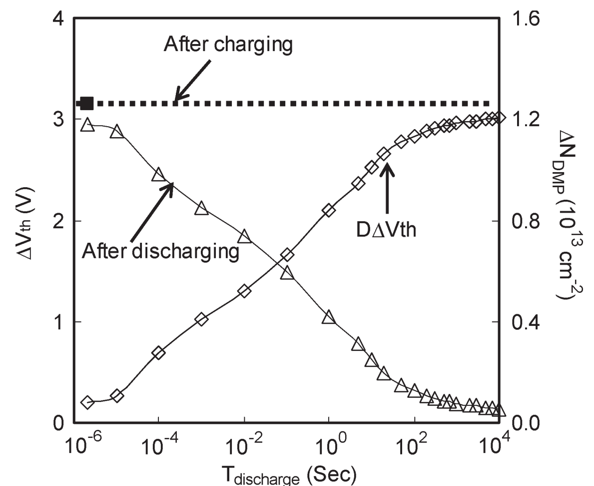
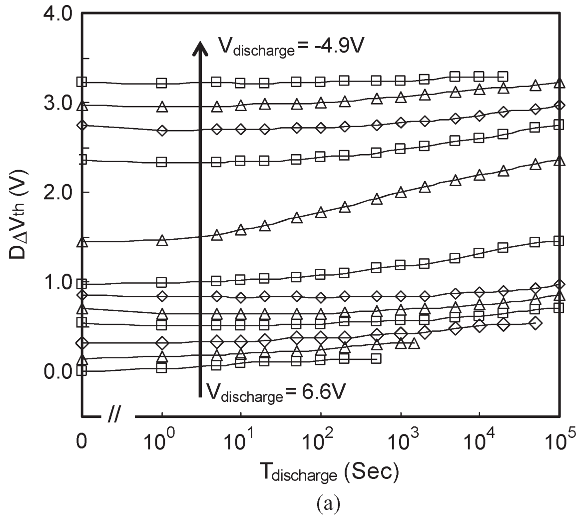


Fig. 5. Trapping level during the discharging of an nMOSFET with 2-nm/10-nm SiON/Al_2O_3 gate stack (stack 2). The device was charged at $V_{\mathrm{charge}} =$ 7 V for $t_{\mathrm{charge}} = 100$ s and then discharged at $V_{\mathrm{discharge}} = -5$ V. $D\Delta V_{\mathrm{th}}$ is their difference. The pulse rising/falling time on the edge is 5 μs. The second Y-axis shows the equivalent discharged trap sheet density at the substrate/dielectric interface ΔN_{DMP}. $V_{\mathrm{discharge}} = -5$ V.



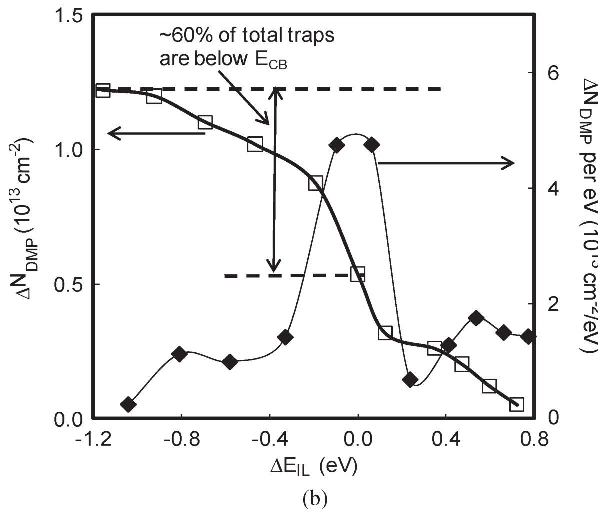
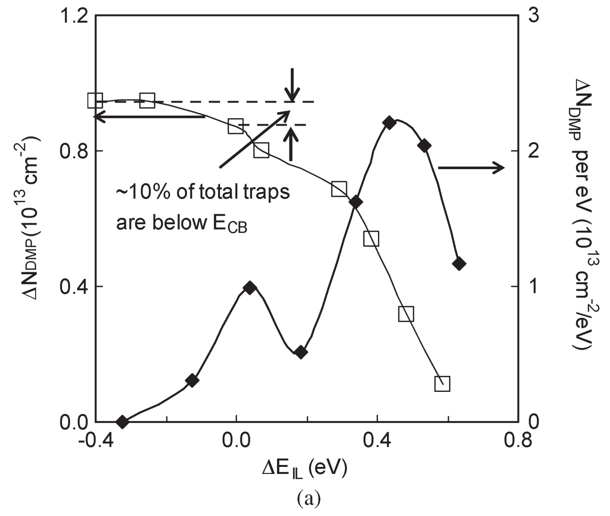


Fig. 6. (a) Typical result of the DMP technique on an nMOSFET with stack 2. The device was charged at a gate bias of 7 V for 100 s to fill the traps before the discharging. (b) Cumulative trap density at the last point of each discharge versus the corresponding energy level and the trap density per electronvolt versus energy level for stack 2. Nearly 60% of the traps in Al_2O_3 are below Si $E_{\rm CB}$. Three peaks are observed at around Si $E_{\rm CB}$, 0.5 eV above Si $E_{\rm CB}$, and 0.8 eV below Si $E_{\rm CB}$, respectively. Only the peak at 0.5 eV can be measured by the CIS technique.



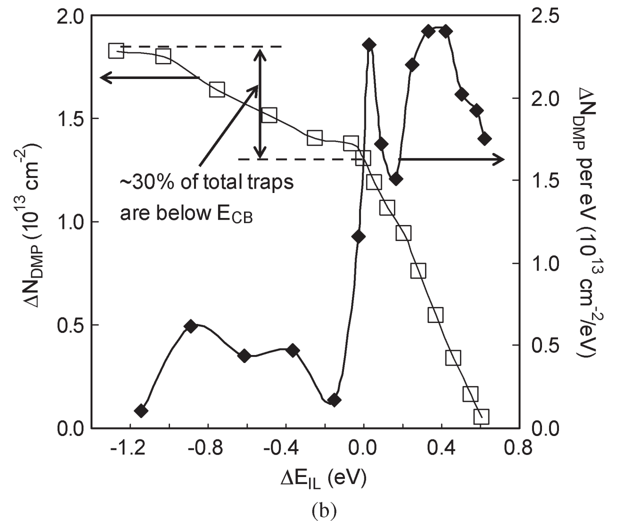


Fig. 7. (a) Cumulative trap density and trap density per electronvolt versus energy level in HfO_2 (stack 4). About 10% of the total traps in HfO_2 are below Si $E_{\rm CB}$. Two peaks are observed at around Si $E_{\rm CB}$ and 0.45 eV above Si $E_{\rm CB}$, respectively. (b) Cumulative trap density and trap density per electronvolt versus energy level in HfAlO (stack 3). About 30% of the traps in HfAlO are below Si $E_{\rm CB}$. Three peaks are observed at around Si $E_{\rm CB}$, 0.45 eV above $E_{\rm CB}$, and 0.9 eV below $E_{\rm CB}$, respectively.

amount of discharge when $\Delta E_{\rm IL}$ is around 0 eV, indicating a high trap density at the energy levels near Si $E_{\rm CB}$.

The $\Delta N_{\rm DMP}$ per electronvolt is also shown in Fig. 6(b) against $\Delta E_{\rm IL}$. The small peak at 0.5 eV above Si $E_{\rm CB}$ agrees well with that extracted by CIS [14]. The large peak near Si $E_{\rm CB}$ and the deeper peak below $E_{\rm CB}$, which could not be extracted by CIS, actually dominate the trapping. These two peaks agree with those observed on Al_2O_3 capacitor samples in our earlier work by using the two-pulse C–V technique [20].

Detailed distributions for HfO_2 and HfAlO are shown in Fig. 7(a) and (b), respectively. Only two peaks are observed in HfO_2. The one at 0.45 eV above Si $E_{\rm CB}$ is dominant, and the one near Si $E_{\rm CB}$ is much smaller. Only 10% of traps in HfO_2 are below Si $E_{\rm CB}$. This means that majority of traps in HfO_2 cannot be probed by the two-pulse C–V technique, demonstrating the advantages of the DMP technique. There are three peaks in the 1:1 cycle HfAlO, with peaks at 0.45 eV above and 0.8 eV below Si $E_{\rm CB}$, respectively. While 70% of traps are above Si $E_{\rm CB}$, the peak at the Si $E_{\rm CB}$ in HfAlO is much higher than that in HfO_2. The normalized energy distributions in HfO_2, HfAlO, and Al_2O_3 are compared in Fig. 8. The trap energy level in Al_2O_3 is clearly deeper than that in HfO_2, and HfAlO combines the features in HfO_2 and Al_2O_3. The deep peak at −0.8 eV in Al_2O_3 and HfAlO agrees well but is missing in HfO_2. HfO_2 has a large shallow peak at 0.45 eV, while Al_2O_3 has a much smaller one. The shallow peak in HfAlO is the average of that in HfO_2 and Al_2O_3. We can therefore conclude that Al induces the deep peak at −0.8 eV and that Hf induces most of the shallow peak at 0.45 eV. This result demonstrates that DMP is capable of identifying the trap energy signature of different high-κ dielectric stacks. Recent retention test in memory cells confirms that higher Hf content results in a larger initial $V_{\rm th}$-window closure, which can be attributed to the fast discharge from its larger amount of shallower traps [22], in agreement with the observation in this paper.

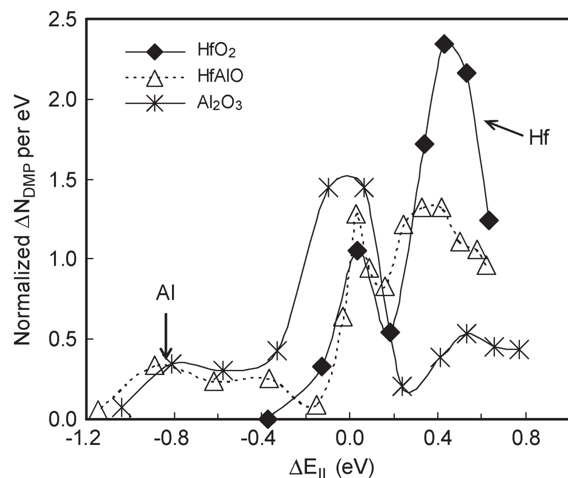


Fig. 8. Comparison of the trap density per electronvolt normalized by the total trap density in gate stacks with Al_2O_3 (stack 2), HfAlO (stack 3), and HfO_2 (stack 4). The area underneath each curve is 1 after the normalization. Al induces the deep peak at -0.8 eV, and Hf induces the shallow peak at 0.45 eV.

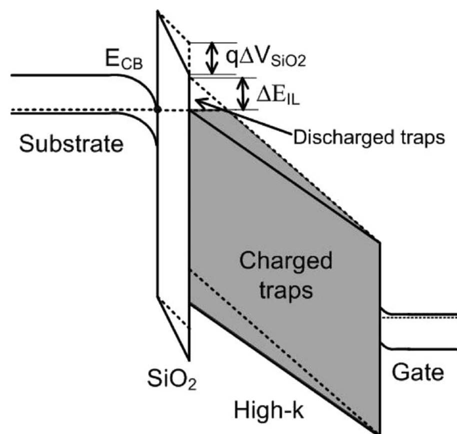
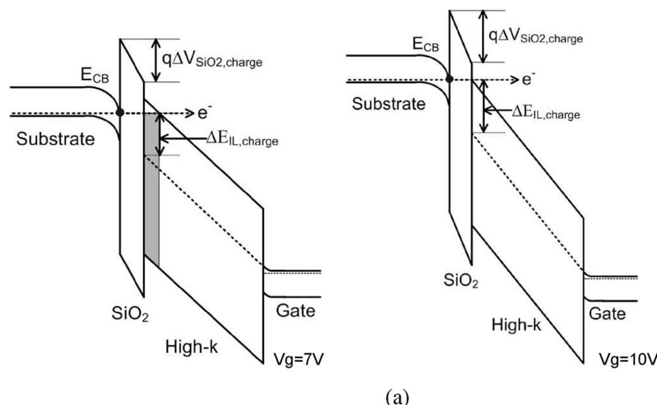
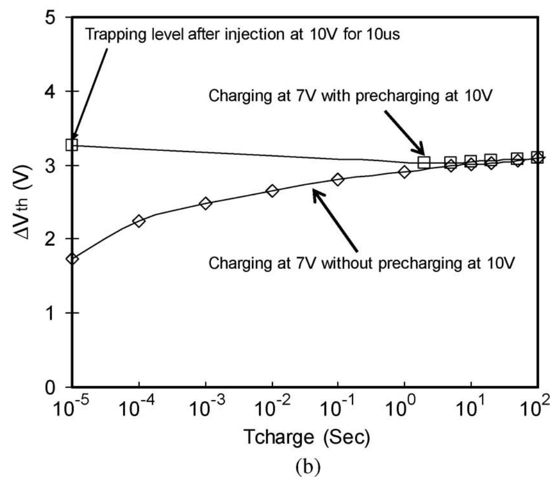


Fig. 9. Energy band diagram of the HfAlO stack (stack 3) at the gate bias of 7 V (solid lines) before and (dashed lines) after the electron trapping. Electrons can be initially injected into the HfAlO's conduction band at the interfacial layer interface and fill the electron traps at all energy levels across HfAlO through scattering. However, electron trapping in HfAlO reduces the effective voltage drop across the interface layer so that the shallower traps in the white region cannot be filled at the end of trap charging.

We now address the trap energy range that can be probed. Fig. 9 shows that the shallowest level is determined by the V_g used to fill the traps. During the trap filling under the positive gate bias, voltage drop across the interfacial layer decreases when the electron trapping in the high-κ layer builds up. It also raises the trap energy level against the Si E_{CB} so that the shallow traps in the white triangle region of the high-κ layer in Fig. 9 can no longer be filled. For the SiON/HfAlO stack (stack 3), the initial voltage drop across the interfacial layer is 2.02 V at a gate bias of 7 V when there is no electron trapping. This allows for the electrons to be injected into the HfAlO's conduction band at the interfacial layer interface and fill the electron traps at all energy levels across HfAlO through scattering. However, as the magnitude of electron trapping in HfAlO is on the order of 10^{13} cm^{-2}, which gives rise to a threshold voltage shift of about 4 V, the effective voltage drop across the interface layer will decrease to 0.71 V at the end of the trap-charging stage. Therefore, the shallow traps at energy level within 1.3 eV below the HfAlO E_{CB} near the interfacial layer interface will rise above the Si E_{CB} and cannot be filled during the trap charging. This gives the shallowest ΔE_{IL} that can be measured by DMP of about 0.7–0.8 eV above Si E_{CB}.





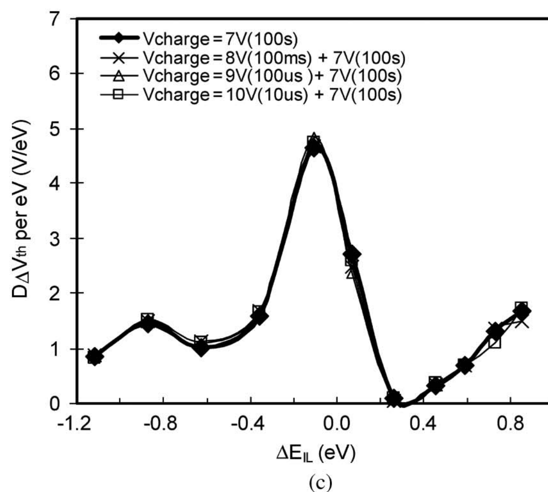


Fig. 10. (a) Energy band diagram of the Al_2O_3 stack (stack 2) before the electron trapping at the gate biases of 7 and 10 V. Electrons cannot be injected into the Al_2O_3's conduction band near the interfacial layer interface at $V_g = 7$ V but can be injected at $V_g = 10$ V. (b) Charging with/without the precharging at 10 V for 10 μs. One device was charged at 7 V for 100 s, and the other one was precharged at 10 V for 10 μs, followed by 7 V for 100 s. (c) There is little difference in the extracted electron trap energy distribution between electron fillings carried out at 7 V for 100 s only, and at 10 V (10 μs), 9 V (100 μs), or 8 V (100 ms) followed by 7 V for 100 s. The effect of the additional injection at higher positive bias is negligible.

In principle, using higher V_g for trap filling will allow probing shallower traps, but a higher V_g can break down the dielectric before trapping saturates, imposing a limit on V_g. The deepest electron trap energy level that has been measured by the DMP technique is at about 1 eV below Si $E_{\rm CB}$. There is no trap deeper than this energy level because all electron traps in the high-κ layer can be discharged when biased at this level (see Fig. 5).

For the Al_2O_3 stack (stack 2), the initial voltage drop across the interfacial SiON layer is 1.73 V for a fresh device without trapping during the trap-filling stage at $V_g = 7$ V. Given the 2.6-eV band offset between the conduction band bottom of Si substrate and the Al_2O_3 layer, electrons do not have enough energy to be injected to the Al_2O_3 conduction band at the SiON/Al_2O_3 interface. They can only be injected into the conduction band in the bulk of Al_2O_3, as shown in Fig. 10(a). This raises the question that whether electron traps near the interfacial layer interface can be filled, as shown in the gray region in Fig. 10(a), and whether this will have significant effects on the extraction of trap energy distribution. To address this potential uncertainty, a large gate bias of 10 V is applied for a short period of 10 μs on a fresh device to inject electrons into the Al_2O_3 conduction band at the IL interface, as also shown in Fig. 10(a), which results in a large trapping density on the order of 10^{13} cm^{-2}. A gate bias of 7 V is then applied for 100 s to ensure the saturation of trapping. As shown in Fig. 10(b), electron injections at 7 V with and without the precharging at 10 V lead to the same trapping level at 100 s, indicating that the effects of the precharging at higher gate bias are small. The extracted energy distributions with and without the precharging are compared in Fig. 10(c), where no significant difference is observed. Similar results are also observed on two other devices with injection at 8 and 9 V followed by 7 V for 100 s. This result indicates that the effects of the electron injection at higher gate bias on the electron trap energy distribution are negligible here, supporting that traps in this gray region in Fig. 10(a) can be filled at $V_g = 7$ V through an inelastic process.

It is also worth noting that $\Delta E_{\rm IL}$ is the trap energy level measured at the SiO_2/Al_2O_3 interface during the discharge. The energy levels of electron traps measured in the bulk are shallower than that at the interface under the positive bias and are deeper under the negative bias. Therefore, the probed energy range varies from $\Delta E_{\rm IL}$ at the IL/high-κ interface to ΔE_G at the high-κ/gate interface, as shown in Fig. 2(c). The trapping density is estimated from the measured $\Delta V_{\rm th}$ in the DMP technique, and its accuracy is affected by the actual trap spatial distribution. To extract the energy distribution at each spatial position, complex modeling and numerical simulation are needed, which are beyond the scope of this paper. Here, we propose a simple method for capturing the "average" energy signature across the high-κ layer by completely discharging traps in the high-κ layer step by step in energy ranges. Since the traps are discharged in energy step by step in the DMP technique, the impact of trap spatial location on the analysis can be limited within a specific energy band, therefore greatly reducing the effects of the convolution between the trap energy level and the spatial location. Further work is needed to take this effect into account when analyzing the detailed energy distribution against their spatial locations, which requires a complex numerical modeling process and is beyond the scope of this paper.

It has been observed that, although annealing condition can affect the trap energy distribution in either Al_2O_3 or HfO_2 stacks, the signature of the trap distribution remains unchanged. Al in dielectric causes deep trap peak around $\Delta E_{\rm IL} = -0.8$ eV, which is always absent in HfO_2. As a result, the DMP technique provides a simple semiquantitative method that can capture the "signature" of the trap energy distribution without complex modeling and simulation, particularly useful when comparing different materials, as shown in Fig. 8. While the technique has limited accuracy, it does reveal the differences in materials; therefore, it can be a useful tool for carrying out fast evaluation during the device development, not only for Flash memory but also for CMOS applications.

IV. Conclusion

A new DMP technique has been developed in this paper, which provides the signature of electron trap energy distribution across the high-κ dielectric layer. Trap energy distributions in HfO_2, Al_2O_3, and HfAlO have been extracted and compared. It has been observed that hafnium is responsible for the shallow traps at about 0.45 eV above the silicon conduction band bottom and that aluminum causes the deep traps at 0.8 eV below the Si $E_{\rm CB}$. HfAlO combines the features in HfO_2 and Al_2O_3. A peak at Si $E_{\rm CB}$ has been observed in all three materials. The DMP technique is a simple tool for capturing the trap energy signature that can assist in material selection during technology development.

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Xue Feng Zheng received the B.Eng. degree and the M.Sc. degree in microelectronics and solid state electronics from Xidian University, Xi'an, China, in 2001 and 2004, respectively, and the Ph.D. degree in microelectronics from the School of Engineering, Liverpool John Moores University, Liverpool, U.K., in 2010.

In 2003, he joined the School of Microelectronics, Xidian University, as a Researcher and became an Assistant Professor in 2010. His research interests include the reliability of MOSFETs, and the degradation and defect characterization of high-κ gate stacks in Flash memory devices.

Wei Dong Zhang received the B.Eng. degree in semiconductor physics and devices from the Beijing Institute of Technology, Beijing, China, in 1989, the M.Sc. degree in semiconductor devices and microelectronics from Xidian University, Xi'an, China, in 1992, and the Ph.D. degree in microelectronics from Liverpool John Moores University, Liverpool, U.K., in 2003.

From 1992 to 1999, he was a Lecturer and then an Associate Professor with the Institute of Microelectronics, Xidian University. In 2002, he joined the Bournemouth University, Bournemouth, U.K., as a Lecturer in microelectronics. In 2005, he joined Liverpool John Moores University as a Senior Lecturer in microelectronics, where he became a Reader in microelectronics in 2010. He has authored or coauthored over 20 journals and conference papers. His current research interests cover the areas of quality and reliability assessment of CMOS and Flash memory devices.

Bogdan Govoreanu (M'05) received the Lic.-Eng. and M.Sc. degrees in electronics from the Technical University (TU) of Bucharest, Bucharest, Romania, in 1995 and 1996, respectively, and the Ph.D. degree in applied sciences from the Katholieke Universiteit Leuven, Leuven, Belgium, in 2004, for his research carried out at the Interuniversity Microelectronics Center (IMEC), Leuven, on novel nonvolatile memory device concepts.

In 1996, he was a Research Assistant with the Electronics Department, TU Bucharest. He is currently with IMEC, where he has been working on various research areas, including modeling, characterization and reliability of nonvolatile/Flash memory, high-κ dielectrics, and TCAD methodologies for empirical model building and optimization techniques. His current research focus is on emerging resistance-switching-based memory concepts. He has published over 60 research papers in internationally recognized journals and conference proceedings and has filed several European and U.S. patent applications.

Jian Fu Zhang received the B.Eng. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 1982 and the Ph.D. degree in electrical engineering from the University of Liverpool, Liverpool, U.K., in 1987.

From 1986 to 1992, he was a Senior Research Assistant with the University of Liverpool, where he worked on the dielectric recovery of plasma in accelerating gas flow, plasma processing of semiconductors, and the reliability of MOS devices. In 1992, he joined Liverpool John Moores University, Liverpool, as a Senior Lecturer, where he became a Reader in microelectronics in 1996 and a Professor in 2001. His current research interests include performance, degradation, and defect characterization of MOS devices and high-κ layers. He has authored or coauthored over 100 journals and conference papers, including ten invited papers at several international conferences.

Dr. Zhang was a member of the technical program committee for the IEEE Semiconductor Interface Specialists Conference.

Jan van Houdt (SM'02) was born in Leuven, Belgium, on June 20, 1963. He received the M.Sc. degree in electrical and mechanical engineering and the Ph.D. degree in applied sciences from the Katholieke Universiteit Leuven, Leuven, in 1987 and 1994, respectively. His M.S. thesis dealt with the degradation of short-channel MOS transistors under hot-carrier injection conditions. His Ph.D. work concentrated on the physics and characteristics of High Injection MOS (HIMOS) Flash memory devices.

After his M.S. thesis, he joined the Interuniversity Microelectronics Center (IMEC), Leuven. In 1990, he invented the HIMOS transistor, a novel fast-programmable Flash EEPROM cell that has led to a high-performance cost-effective nonvolatile memory technology, on which he holds numerous international patents. In 1996, he became responsible for the development and dissemination of Flash memory technology based on IMEC's proprietary concepts, including the licensing and the transfer of these technologies toward four industrial product lines. Since 1999, he has been managing the memory group at IMEC. From 2000 to 2008, he also managed IMEC's Industrial Affiliation Program on Advanced Memory Technology and expanded it to become one of IMEC's largest research programs today. His research interests are physics of semiconductor devices, hot-carrier injection and degradation phenomena in MOS structures, thin dielectrics, modeling and optimization of floating-gate and nitride nonvolatile memory devices, reliability physics and design aspects of memories in general, the application of high-κ materials in novel memory devices, and emerging nonvolatile memory concepts such as resistance RAM. He has published more than 160 papers in international journals, written two book chapters, and accumulated more than 140 conference contributions (including more than 20 invitations and four best paper awards). He has filed about 45 patent applications worldwide in the area of nonvolatile memories, out of which 24 patents have been granted so far.

Dr. van Houdt serves (or served) on the program and/or organizational committees of the IEEE Nonvolatile Semiconductor Memory Workshop, the IEEE Reliability Physics Symposium, the European Solid-State Device Research Conference, the International Conference on Memory Technology and Design, the IEEE International Workshop on Memory Technology, Design and Testing (Taiwan), the Solid-State Devices and Materials conference, the MRS symposium on nonvolatile memory technologies, and the IEEE International Electron Devices Meeting. In 2007, he was the General Chairman of the International Conference on Memory Technology and Design. He was the recipient of the Best Student Paper Award at the 22nd European Solid-State Device Research Conference in 1992 and the Scientific Award of the Royal Academy for Science, Literature and Fine Arts of Belgium in 1995.