

A Novel Trapping/Detrapping Model for Defect Profiling in High- k Materials Using the Two-Pulse Capacitance–Voltage Technique

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Abstract—The continuous reduction of the dimensions of floating-gate-based nonvolatile memories brings the necessity of substituting the current dielectrics with materials of higher dielectric constant (high- k dielectrics). However, most of the high- k materials studied show a large number of electrically active defects, which mitigates their benefit. The study of these defects, or traps, is necessary in order to fully understand the electrical properties of high- k materials. In this paper, the recently introduced two-pulse capacitance–voltage characterization technique is used, together with a newly developed physics-based model, in order to extract the space and energy location of the traps throughout the high- k dielectrics in advanced memories. An accurate agreement between measurements and simulations is achieved. For the first time, it is shown that traps located in the top part of the bandgap of the high- k materials can be probed and their location in space and energy, as well as their density, can be accurately determined.

Index Terms—High- k dielectrics, nonvolatile memories, semiconductor device modelling.

I. INTRODUCTION

THE SCALING-DOWN of Flash memory technology to sub-45-nm nodes may require cell planarization due to the lack of physical space between two neighboring cells; hence, a considerable reduction of the electrical thickness of the interpoly dielectric (IPD) is required in order to compensate for the loss of the sidewall coupling capacitance [1]. This is achievable by combining high- k IPDs with high-work-function metal gates [1]–[3]. Even if the coupling capacitance is thus restored, the devices with high- k -based IPDs exhibit a performance loss due to the large number of defects present in the new materials [4]. The electrical properties of these defects must be known in order to estimate their impact on the electrical behavior of the device and eventually understand their nature.

Several attempts have been made to characterize the defects [5]–[8], but the methods proposed so far have limited energy and spatial resolution, either dictated by fundamental or practical limitations. A low-frequency charge-pumping technique

[9]–[12] measures a recombination current that is proportional to the applied pulse frequency. In order to sense traps located farther away from the interface, the pulsewidth and period must increase, thus reducing the frequency. The minimum frequency that can be used is around 0.1 Hz using an electrometer to directly measure the pumped charges [10], giving a tunneling time of less than 10 s, which means that around up to two nanometers of the dielectric stack can be scanned [11].

The TSCIS technique [13] tries to solve this limitation by measuring the threshold voltage variation of a transistor when injecting charges into the dielectric. In this case, the scanned region will depend on the injection time. An injecting time of 10^4 s allows scanning for as far as around 3 nm inside the dielectric. However, scanning energies below the silicon conduction band is not possible since elastic injection is assumed, and scanning energies above the silicon conduction band is also limited by the need to avoid leakage through the whole dielectric stack.

Pulsed I_d – V_g methods for extracting the density and location of the traps are also based on monitoring the variations of V_T after the charging of the traps present on the dielectric stack of a transistor [14]. However, the measurement setup and methodology require a fine tuning, and the energy range scanned is quite limited.

This paper presents the new two-pulse capacitance–voltage (CV) measurement technique, based on monitoring the discharge of defects under different bias conditions [15], which, together with a new trapping/detrapping model, allows the extraction of the density and location, in space and energy, of the defects over a much larger part of the dielectric bandgap with respect to the techniques mentioned before.

This paper is organized as follows. Section II presents a description of the test structures used in the experimental part. In Section III, the two-pulse CV method will be reviewed. The theoretical model used to simulate the trapping/detrapping conditions of the dielectric stack is presented in Section IV. Section V presents the comparison of simulations and experimental results. Finally, the impact of different parameters used in the model will be studied in Section VI, in order to gain more insight on the trapping/detrapping kinetics of different traps. The main conclusions are summarized in Section VII.

II. DEVICE DESCRIPTION

The test structures used in this work are MOS capacitors, as shown schematically in Fig. 1(b). The dielectric stack of these

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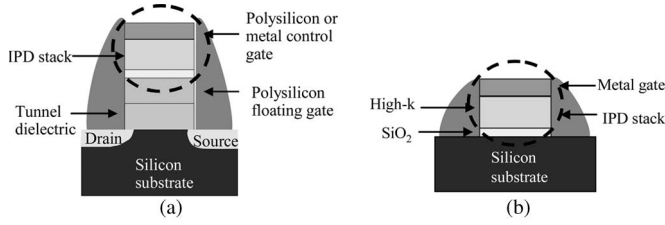


Fig. 1. Schematic drawing of (a) a floating-gate transistor with a high-*k*-based IPD stack and (b) the capacitor used in this work, which uses the IPD stack as dielectric. The stack dielectric is formed by a bottom interfacial SiO₂ layer and a top Al₂O₃ layer.

capacitors is similar to a high-*k*-based IPD stack of a floating-gate transistor [Fig. 1(a)], except for the layer thicknesses which have been adjusted in order to improve the robustness of the experimental data. The gate stack is deposited on an n-type Si substrate and is formed by a 2 nm of ISSG silicon dioxide and 6 nm of Al₂O₃ deposited by atomic layer deposition using trimethyl aluminum (Al(CH₃)₃ or TMA) and water as precursors. The entire stack received a postdeposition anneal (PDA) at 1000 °C for 60 s in a N₂ atmosphere. This PDA step crystallizes the Al₂O₃ layer and produces a reduction in thickness of about 15% [16]; thus, the final thickness of the Al₂O₃ layer is ~5.2 nm. A TiN gate is deposited using ionized metal plasma sputtering process [17]. From the *CV* measurements, the value of the relative dielectric constant of Al₂O₃ is calculated as $k_{\text{Al}_2\text{O}_3} = 9.5$.

III. MEASUREMENT PRINCIPLE

The pulse *CV* technique [18] allows performing fast measurements of the *CV* characteristic of a device by monitoring the gate current of the capacitor. The definition of the current *I* of a capacitor *C* when applying a variable voltage dV/dt is

$$I = C \frac{dV}{dt} \Rightarrow C = \frac{1}{\frac{dV}{dt}} I. \quad (1)$$

A gate voltage pulse with constant slope *A* gives

$$\frac{dV}{dt} = A \Rightarrow C = \frac{I}{A}. \quad (2)$$

Therefore, measuring the displacement current through the capacitor allows obtaining the *CV* curve of a MOS device. The measurement setup is schematically shown in Fig. 2: A pulse generator is connected to the gate of the capacitor; when a pulse is applied, the displacement current at the bulk is first amplified and then transformed into a voltage signal by a transconductance in order to be measured by an oscilloscope.

A typical output of this setup is shown in Fig. 3(a). The *CV* curves obtained during the leading and trailing edges of the pulse are identical only if there was no trapping of charges during the top level of the pulse. However, when applying a pulse with high-enough top level, charges can be trapped inside the dielectric, and the *CV* curve is shifted as shown in Fig. 3(b). The trailing curve shifts to the right with respect to the initial leading curve, indicating that a net negative charge has been trapped inside the dielectric. The kink observed on the leading curve of Fig. 3(b) at V_g smaller than V_{FB} is caused by the slow

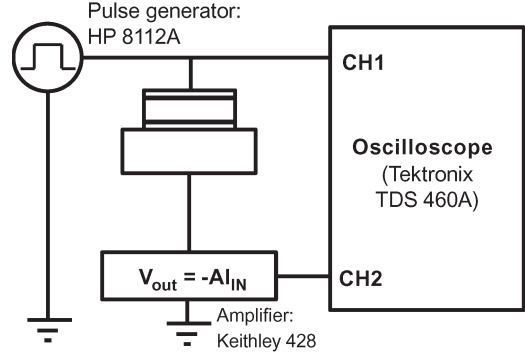


Fig. 2. Pulse *CV* setup. A pulse generator is connected to the gate of a capacitor. The displacement current at the bulk is amplified and transformed into a voltage signal. An oscilloscope measures the obtained voltage signal together with the applied pulse.

recombination of the minority carriers (holes) injected into the substrate from the inversion layer.

The basic principle of the two-pulse *CV* technique [15] is shown in Fig. 4. The discharging rate of the traps can be monitored by keeping the capacitor biased at a constant gate voltage V_{base} for a certain discharge time t_{dis} between two consecutive gate pulses. The total discharge is obtained from the flatband voltage shift ΔV_{FB} between the trailing trace of the first pulse and the leading trace of the second pulse. The flatband voltage measured on the trailing traces is practically constant for both applied pulses, indicating that no extra defects are generated during the measurement. The flatband voltage measured on the trailing traces will be denoted as $V_{\text{FB, charged}}$. The measured ΔV_{FB} is defined throughout this paper with respect to $V_{\text{FB, charged}}$, so a positive ΔV_{FB} indicates that the *CV* curve has shifted toward lower V_{FB} . The ramp rate for the rise/falling edges has been fixed to 10 kV/s, leading to rise/fall times of 100 μs for each 1 V of difference between the two voltage levels ($V_{\text{base}}, V_{\text{top}}$). This value has been experimentally found as a best compromise for our setup: Slower ramp rates will cause more trapping/detrapping during the *CV* measurements, while higher ramp rates are limited by the transamplifier's bandwidth.

The measured ΔV_{FB} is specific for each t_{dis} and V_{base} , and a model has been developed in order to simulate those detrapping conditions. The measurements will be used to confirm the theoretical detrapping rates obtained. The fitting of measurements with the model allows extracting all the trap parameters, i.e., their density, location, and energy.

In this paper, ΔV_{FB} is measured for t_{dis} between 10 ms and 5000 s and for different V_{base} from 0.8 to -4.8 V with a voltage step of -0.4 V. A typical output of the procedure is shown in Fig. 5, where the ΔV_{FB} curves obtained are assumed to be caused only by trapping or detrapping of electrons since the n-type substrate of the devices minimizes the possible hole injection during the measurements. Fig. 5 will be further discussed in Section VI.

IV. TRAPPING/DETRAPPING MODEL

A physics-based model has been developed in order to fully understand the detrapping dynamics observed with the two-pulse *CV* technique. The variation of V_{FB} with the time and

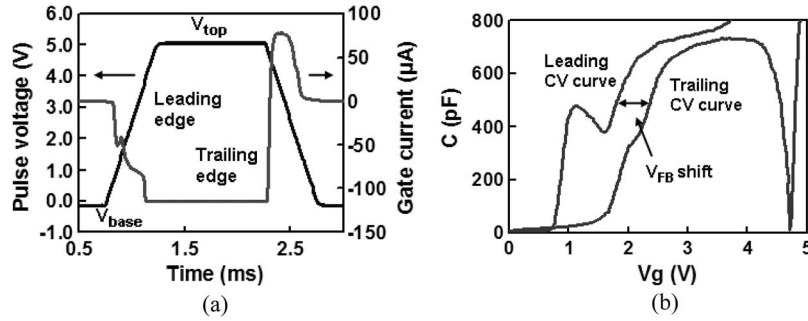


Fig. 3. (a) Output of the pulse CV setup and (b) the final CV curves obtained. The shift of the trailing curve with respect to the initial leading curve indicates that charges have been trapped inside the dielectric during the top part of the pulse.

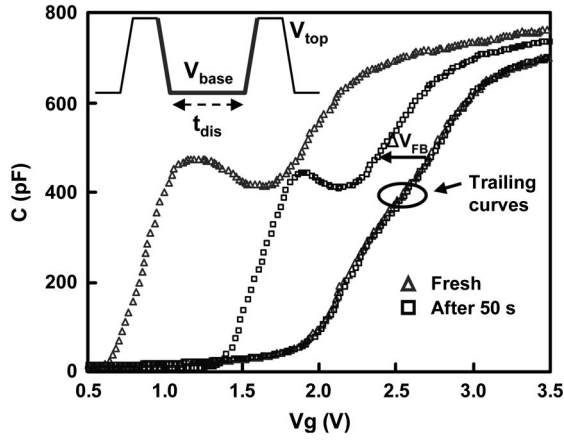


Fig. 4. CV curves obtained with the two-pulse CV technique. The fresh curve is compared with the one after a discharge time $t_{dis} = 50$ s. $V_{top} = 5$ V, $V_{base} = -1$ V, and the pulsewidth at V_{top} is 1 ms. The ramp rate is 10 kV/s.

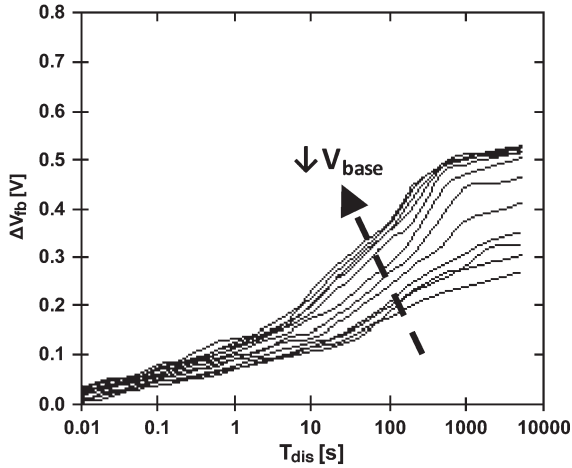


Fig. 5. ΔV_{FB} obtained with the two-pulse CV technique using the devices described in Section I. The discharge time t_{dis} varies between 10 ms and 5000 s, and V_{base} ranges from 0.8 to -4.8 V with a step of -0.4 V.

the applied bias depends on the traps that are emptied or filled with electrons under those conditions. Thus, the total variation of charge density inside the dielectric can be calculated as

$$\frac{dn_T(z, E, t)}{dt} = N_T(z, E) \cdot [1 - f_T(z, E, t)] \cdot \frac{1}{\tau_c(z, E)} - N_T(z, E) \cdot f_T(z, E, t) \cdot \frac{1}{\tau_e(z, E)} \quad (3)$$

where $n_T(z, E, t)$ is the density of charged traps at each spatial location z , energy position E , and time t ; $N_T(z, E)$ is the total density of traps; and $\tau_c(z, E)$ and $\tau_e(z, E)$ are the capture and the emission times of each trap location, respectively. The trap occupation probability in the transient regime $f_T(z, E, t)$ gives the probability of a trap being charged under certain bias conditions for a period t .

The density of charged traps is given by the trap density multiplied by the trap occupancy probability, i.e., $n_T(z, E, t) = N_T(z, E) \cdot f_T(z, E, t)$. Considering that no significant defect generation takes place during the experimental procedure, the trap density is assumed to be time independent, which allows one to rewrite (3) as follows:

$$\frac{df_T(z, E, t)}{dt} = \frac{1 - f_T(z, E, t)}{\tau_c(z, E)} - \frac{f_T(z, E, t)}{\tau_e(z, E)}. \quad (4)$$

With further assumption of the time-independent capture and emission times for a particular space-energy location, (4) integrates to

$$f_T = f_T(0) \cdot e^{-\frac{t}{\tau}} + \frac{\tau}{\tau_c} \cdot \left(1 - e^{-\frac{t}{\tau}}\right) \quad (5)$$

where τ has been defined as $\tau = (\tau_c \cdot \tau_e) / (\tau_c + \tau_e)$.

From (5), it is clear that in order to calculate the occupancy probability, it is sufficient to calculate τ_c and τ_e and to know the initial distribution of the trapped charge, described by the trap occupancy probability function $f_T(0)$. The capture times τ_c 's are calculated according to [19], with a capture process from the carrier supply to the trap assuming inelastic tunneling, where a number of phonons are emitted as a consequence of the carrier energy relaxation in the trap potential well [20]. The detrapping (emission) times from the traps toward electrodes are calculated by assuming quasi-elastic detrapping taking place from the trap energy level, hence neglecting possible phonon absorption before tunneling out of the traps. This simplification turned out to not affect significantly the accuracy of the calculation, provided that the traps considered are not too shallow (below 1-eV depth). The emission time of a trap is inversely proportional to the tunnel-out probability of the trapped charge T_{escape} calculated using the Wentzel-Krammer-Brillouin approach [21]

$$\tau_e = \frac{\tau_{trap}}{T_{escape}} \quad (6)$$

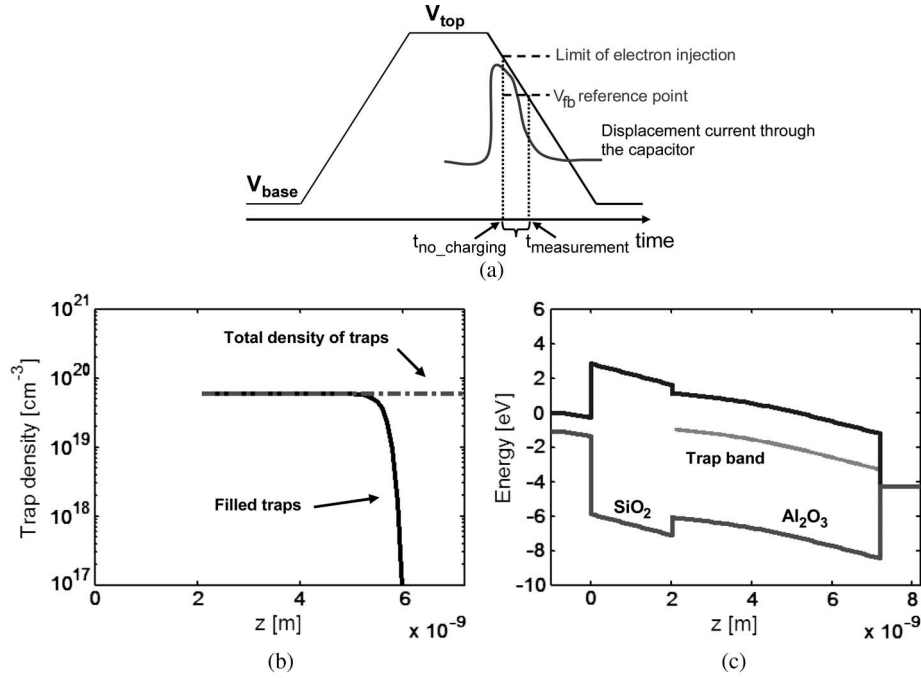


Fig. 6. (a) Applied pulse edge, (b) calculated initial conditions of trapped charge, and (c) band diagram when the structure is biased at $V_{\text{no_charging}}$. A uniform distribution of defects has been considered between 2 and 2.2 eV below the high-*k* conduction band.

where τ_{trap} is a time constant [22]–[24] and the tunnel probability is given by

$$T_{\text{escape}} = \exp \left(-2 \cdot \int_0^z \sqrt{\frac{2 \cdot m_e^*}{\hbar^2} \cdot q_e \cdot (E(z) - E_{\text{Trap}})} \right) \quad (7)$$

where \hbar is the reduced Plank constant; m_e^* is the electron effective tunneling mass in the corresponding material; q_e is the electron charge; $E(z)$ is the tunnel barrier potential energy, which depends on the applied bias, band offsets, and the charge trapped in the dielectric stack; and E_{Trap} is the energy level of the considered trap. When calculating $E(z)$, apart from the applied bias, the model takes into account the potential distortions caused by the trapped charges into the dielectric bandgap. The trapped charge creates an internal electric field, and thus, it modifies the potential energy profile across the stack. For a given density of charge $\rho(z) = n_T(z) \cdot q_e$, the potential $V(z)$ is given by Poisson's equation

$$\frac{d}{dz} \left(k(z) \frac{dV}{dz} \right) = -\frac{\rho(z)}{\varepsilon_0} \quad (8)$$

where $k(z)$ is the relative dielectric constant of the material, which varies over the distance if different materials are present in the stack, and ε_0 is the vacuum permittivity.

For a given applied bias, the trapped charge can detrapp either toward the gate or toward the substrate, depending on the charge-induced potential energy profile across the stack; therefore, (7) is applied twice for calculating the escape probability of electrons toward the gate and toward the substrate.

In order to specify the initial occupancy probability function $f_T(0)$, the nonideality of the pulse edges is taken into account.

Since the pulse edges are not instantaneous, the charge can be trapped or detrapped during the pulse edge time, as shown in Fig. 6(a). At the beginning of the trailing edge of the first pulse, all the traps are considered charged. During the trailing edge of the pulse, the voltage that does not produce more electron injection, i.e., $V_{\text{no_charging}}$, is achieved at time $t_{\text{no_charging}}$. The voltage $V_{\text{no_charging}}$ can be easily extracted by studying the maximum pulse amplitude that does not produce any shift in two consecutive *CV* curves. Therefore, after the time $t_{\text{no_charging}}$ and until the time where V_{FB} is measured, i.e., $t_{\text{measurement}}$, only detrapping occurs. By using a voltage slope of 10 kV/s, the lapse of time is on the order of $\sim 100 \mu\text{s}$ for the structures considered in this paper. These conditions define how many traps remain charged when $V_{\text{FB, charged}}$ is measured and thus define the initial occupancy probability function $f_T(0)$. Fig. 6(b) shows an illustrative density of traps and the quantity of filled traps when V_{FB} is measured in the MOS capacitor structure described in Section II. The band diagram of the structure biased at $V_{\text{no_charging}}$ is shown in Fig. 6(c).

In order to obtain the initial density of traps and the band diagram in Fig. 6(b) and (c), the following were assumed for the SiO_2 and Al_2O_3 , respectively: *k* values of 3.9 and 9.5, relative electron masses of 0.48 and 0.35, and conduction band offsets relative to the conduction bands of the Si substrate of 3.1 and 2.6 eV. The doping of the Si substrate is 10^{15} cm^{-3} , and the work function of the TiN metal gate is 4.6 eV. These parameters will be used in the rest of the work to define the $\text{SiO}_2/\text{Al}_2\text{O}_3$ stacks.

Fig. 7(a) shows the schematized trapping/detrapping paths of the charge for different V_{base} values, and Fig. 7(b) shows the evolution of the occupation factor f_T with time when $V_{\text{base}} = -2 \text{ V}$. It is observed that, at very short times, the detrapping is mainly toward the gate, except for the very shallow traps.

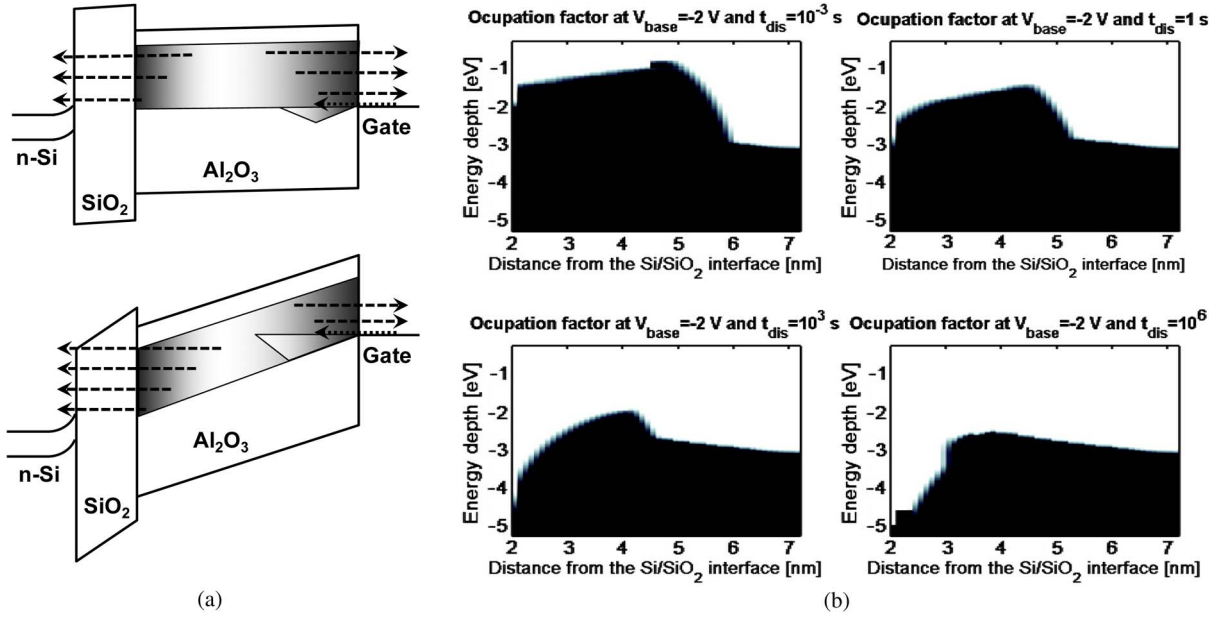


Fig. 7. (a) Schematized trapping/detrapping processes at (top) $V_{base} = 0$ V and (bottom) $V_{base} = -2$ V. The time of the charge to detrapp (or to get trapped) is shorter in the darker regions. The amount and length of the arrows indicate how easy it is for the charge to detrapp (or to get trapped), and it can be toward the substrate or toward the gate depending on the location of the charge and the applied voltage. The triangles indicate the area where trapping is more likely to occur during the measurements. (b) Occupation factor at $V_{base} = -2$ V for different discharging times. The black color means that the trap at that location is filled with electrons, whereas white color means that the trap is empty. The energies are related to the conduction band bottom of the high- k material. The work function of the metal gate is 3 eV below the conduction band bottom of the high- k material. The considered structure is shown in Fig. 6(c). Only the high- k layer is shown since no traps are considered in the SiO_2 layer.

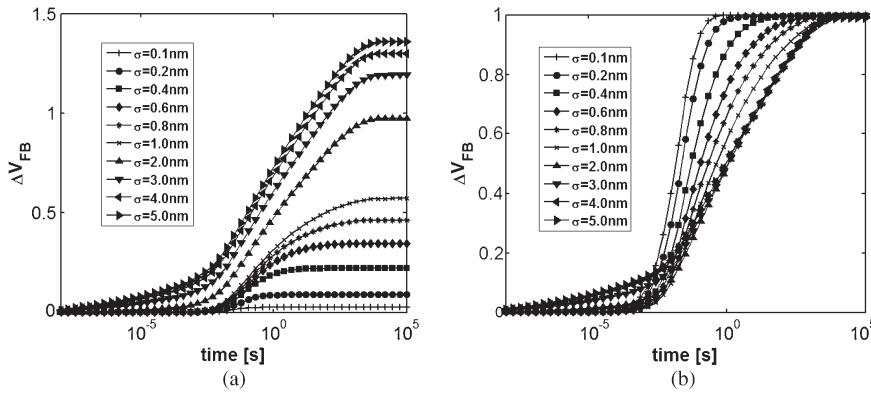


Fig. 8. V_{FB} variation caused by traps with different spatial distribution versus time. The traps have been uniformly located between 2 and 2.2 eV below the conduction band edge of the high- k layer. The density in the center of the Gaussian distribution, located at the SiO_2 /high- k interface, is (a) constant at $6 \times 10^{19} \text{ cm}^{-3}$ or (b) calculated in order to produce a maximum variation of $V_{FB} = 1$ V. No traps are considered in the SiO_2 layer. The detrapping voltage V_{base} is -2 V.

Afterward, detrapping toward the substrate becomes dominant. Traps deeper than 4 eV and located close to the SiO_2/Al_2O_3 interface can be detrapped, and thus sensed, due to the cantilever effect produced by the SiO_2 layer, which pushes the traps above the conduction band of the Si substrate as shown in Fig. 7(a).

Once the profile of the trapped charge across the structure $n_T(z)$ at certain time is known, the corresponding flatband voltage variation is calculated as

$$\Delta V_{FB} = - \int_0^{d_{stack}} q_e \frac{z \cdot n_T(z)}{k(z) \cdot \epsilon_0} dz \quad (9)$$

where d_{stack} is the total thickness of the dielectric stack.

V. STUDY OF THE TRAPPING/DETRAPPING DYNAMICS

In this section, the capture and emission dynamics of carriers from traps located in the Al_2O_3 layer or the SiO_2/Al_2O_3 interface will be studied using the model introduced in the previous section. Different parameters will be considered, such as the spatial and energy distribution of the traps or the thickness of the SiO_2 layer.

Fig. 8 shows the impact of the spatial distribution of traps on the simulated ΔV_{FB} versus time. The spatial distribution of traps is assumed Gaussian, with the central value of the distribution corresponding to the SiO_2 /high- k interface. Furthermore, the half of the profile that locates in the SiO_2 has been set to zero, since the oxide was assumed trap free for simplicity. The maximum density of traps in the center of the Gaussian

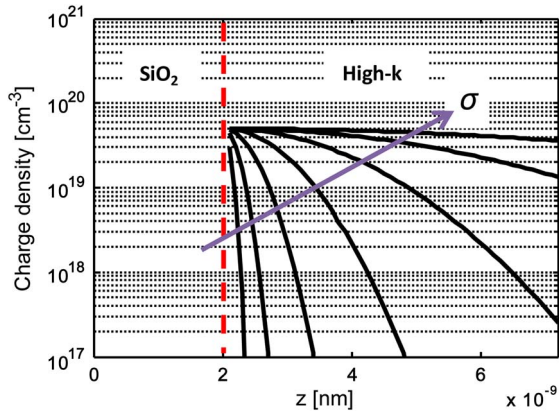


Fig. 9. Charge density in a high-*k* layer distributed in space using a Gaussian profile centered in the SiO₂/high-*k* interface. Different standard deviations σ 's have been used from 0.1 to 6.4 nm with a factor of 2.

distribution is either fixed, as in Fig. 8(a), or calculated in order to produce a maximum flatband voltage shift of 1 V, as in Fig. 8(b). It has been assumed that the traps are located between 2 and 2.2 eV below the conduction band edge of the high-*k* layer. This energy depth has been chosen since the detrapping is observed in a practical time scale; too shallow defects would detrapp too fast, and too deep defects would detrapp too slowly. Moreover, all the traps are considered charged at the beginning of the simulation. The detrapping voltage is -2 V.

A different standard deviation σ of the Gaussian profile indicates how much the traps extend inside the high-*k* layer. This form of trap distribution has been selected for convenience, as it allows compactly describing an interfacial density as well as a quasi-uniform density with a single mathematical formulation. Thus, a deviation of 0.2 nm or lower corresponds to interfacial traps, whereas a deviation of 4 nm or higher can be well approximated by a uniform profile across the film as shown in Fig. 9.

It is shown in Fig. 8 that the slope of the ΔV_{FB} curves decreases when the traps are more spread across the dielectric layer. This is attributed to the fact that charge trapped farther away from the interface will need more time to detrapp. The differences in the saturation point of the ΔV_{FB} curves in Fig. 8(a) are caused by the different $V_{FB, charged}$ obtained when varying the spread of the Gaussian profile. The larger the deviation, the more traps are located in the bulk of the high-*k* layer and, therefore, the larger the $V_{FB, charged}$. Moreover, when increasing the spread of the Gaussian distribution above 1 nm, the discharge starts earlier in time. This is produced by detrapping of bulk traps toward the gate, as shown in Fig. 7(a). A further spread in the distribution of traps means that more traps are located closer to the gate, so an increase in that initial detrapping is observed. However, the saturation point of the ΔV_{FB} curves with a standard deviation larger than 2 nm is constant in Fig. 8(a) and (b), since it is limited by the charges detrapping toward the substrate. A further increase of the spread in space will correspond to more traps in the bulk that will detrapp faster toward the gate.

The ΔV_{FB} curve produced by a uniform distribution (with a standard deviation of > 5 nm) in the structures considered in this work typically presents four different regions. The first re-

gion consists of an initial slow V_{FB} variation caused by charges very close to the gate being detrapped toward the gate. Later, there is a strong acceleration in the V_{FB} variation due to charges being discharged to the substrate in addition to the charges being discharged to the gate. The third region is characterized by a slight decrease in the ΔV_{FB} slope since detrapping toward the gate reaches saturation and the ΔV_{FB} is caused only by detrapping toward the substrate. Finally, saturation is achieved when all the charges have been detrapped from the dielectric stack.

The impact of the energy depth of the traps in the ΔV_{FB} curves is shown in Fig. 10, for both a uniform spatial distribution of traps and interfacial traps located at the SiO₂/high-*k* interface. It is observed that, for the interfacial traps [Fig. 10(b)], the discharge curves remain parallel, although shifted, to longer times when increasing the energy depth. However, for the uniform distributions [Fig. 10(a)], the discharge curves change more drastically; the slope of the discharge curve not only shifts toward longer times but also varies together with the saturation level of the discharge. This is caused by the balance between trapping of electrons from the gate and detrapping of electrons mainly toward the substrate, as shown in Fig. 7(a). This process slows down the net detrapping speed and eventually reaches a stationary state corresponding to a fraction of traps being charged. Fig. 10(a) includes a dotted and a dashed curve obtained with the model when the trapping of charge coming from the gate is not considered. It is observed that both the saturation level (for shallower levels) and the ΔV_{FB} variation over the whole time scale (for deeper levels) can be miscalculated if the trapping from gate injection is not included in the model. The effect of the gate trapping mechanism depends therefore on the depth of the traps assumed in the high-*k* dielectric and also on the discharge gate bias (not shown).

Fig. 11 shows the impact of the applied V_{base} on the ΔV_{FB} curves for interfacial traps at two different energy locations. It is observed that a more negative V_{base} causes an earlier detrapping, in this case toward the substrate; however, the impact of the V_{base} decreases when considering deeper traps in energy. This last result is explained by the lower relative variation of the potential barrier caused by the applied gate voltage when the traps are located farther from the conduction band edge.

The impact of the thickness of the SiO₂ layer on the ΔV_{FB} curves is shown in Fig. 12. A uniform distribution of 6×10^{19} cm⁻³ located between 2 and 2.2 eV below the bottom of the conduction band of the high-*k* layer is considered. A different V_{base} is applied in each simulation, in order to obtain the same electric field in the SiO₂ layers. The electric field in the SiO₂ layer is kept constant, so the differences observed in the ΔV_{FB} curves are caused only by the different thicknesses of the SiO₂ layer and not due to a different potential barrier. The inset in Fig. 12 shows the detrapping path of the charges through a SiO₂ layer with different thicknesses at a constant electric field. The traps need longer times to emit the charge when the thickness of the SiO₂ increases. However, when the detrapping electrons enter the conduction band of the SiO₂, a further increase in the thickness of this layer has little or no impact on the detrapping process.

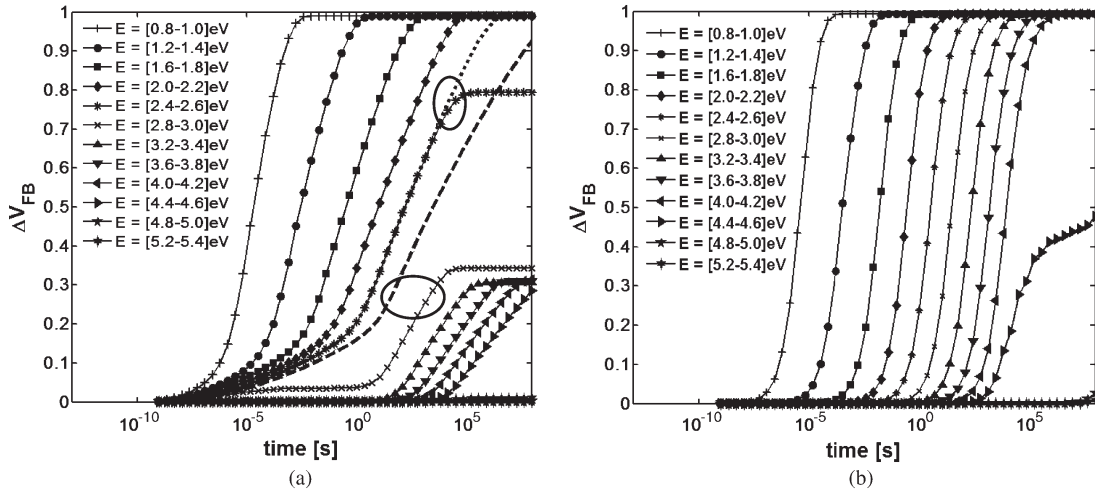


Fig. 10. V_{FB} variation caused by traps at different energy depths versus time. The traps are (a) uniformly distributed with a density of $4 \times 10^{19} \text{ cm}^{-3}$ or (b) located at the $\text{SiO}_2/\text{high-}k$ interface with a density of $1.2 \times 10^{13} \text{ cm}^{-2}$. The detrapping voltage is $V_{base} = -2 \text{ V}$. The dotted and dashed lines in (a) are simulated, not considering the trapping mechanism.

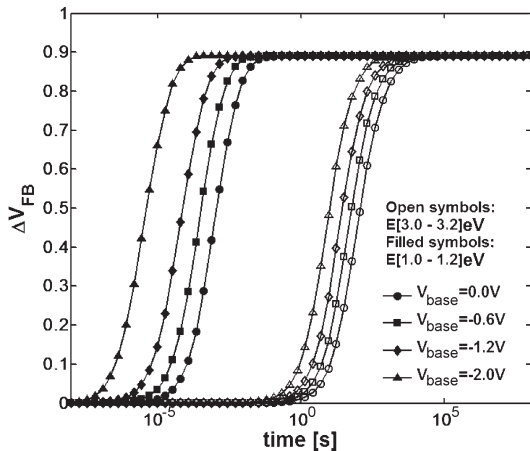


Fig. 11. V_{FB} variation caused by traps at different energy depths and for different applied voltages versus time. The traps are located at the $\text{SiO}_2/\text{high-}k$ interface with a density of $1.2 \times 10^{13} \text{ cm}^{-2}$.

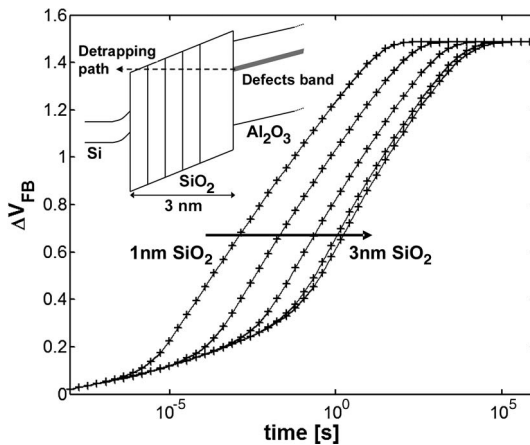


Fig. 12. V_{FB} variation caused by traps in a structure with different SiO_2 layer thickness versus time. The traps are uniformly distributed in space with a density of $6 \times 10^{19} \text{ cm}^{-3}$ and between 2 and 2.2 eV below the conduction band bottom of the high- k . The SiO_2 thicknesses vary from 1 to 3 nm with a thickness step of 0.5 nm. The electric field in the SiO_2 layer is kept constant. The inset represents the different structures considered, under the same electric field, and the detrapping path for the charges.

VI. TRAP DISTRIBUTION IN CRYSTALLINE Al_2O_3

The results obtained with the two-pulse CV technique shown in Fig. 5 are used to calibrate the physical model. It is observed that the ΔV_{FB} curves present three different regions. The first region, until $t_{dis} < \sim 10 \text{ s}$, shows a moderate detrapping rate for all V_{base} voltages. The second region, $t_{dis} > \sim 10 \text{ s}$, presents a change in the ΔV_{FB} slope, which is more pronounced as V_{base} becomes more negative. These two different detrapping regions are caused by two different kinds of traps as will be shown later. The third region, for $t_{dis} > \sim 1000 \text{ s}$, shows again a lower slope in the ΔV_{FB} curves for large negative V_{base} , indicating that the electrons are detrapping much slower from the dielectric. In the measurement shown in Fig. 5, $V_{FB, charged}$ is 0.72 V, whereas the saturation is produced at $\Delta V_{FB} = \sim 0.6 \text{ V}$. This means that not all the charges in the dielectric can detrapp during the experiment, indicating that traps that are deeper than 5 eV below the conduction band bottom of the Al_2O_3 may be present in the layer.

The detrapping constant used in (6), i.e., τ_{trap} , is different for each material. The trap distributions obtained in [13] and [25] for similar structures using $\text{SiO}_2/\text{Al}_2\text{O}_3$ dielectrics were used in order to adjust the value of the detrapping constant. Those results show traps distributed between 1.6 and 2.2 eV below the conduction band edge of the high- k dielectric. The Al_2O_3 dielectrics used in memory devices show low-temperature activation [26]; therefore, it is assumed that there are little or no traps at energy depths of less than 1 eV. Thus, the traps situated between 1.6 and 2.2 eV are considered the shallowest in the Al_2O_3 layer, and they cause the initial detrapping shown in Fig. 5 for $t_{dis} < \sim 10 \text{ s}$. Indeed, this first part of the ΔV_{FB} curve can be fitted with our model when considering a spatially uniform distribution of traps normally distributed in energy with the central level at 1.8 eV below the high- k conduction band edge when the detrapping time constant $\tau_{trap} = 5 \times 10^{-10} \text{ s}$. The standard deviation of this shallow trap distribution is 0.1 eV. The first part of the experimental detrapping curves, which corresponds

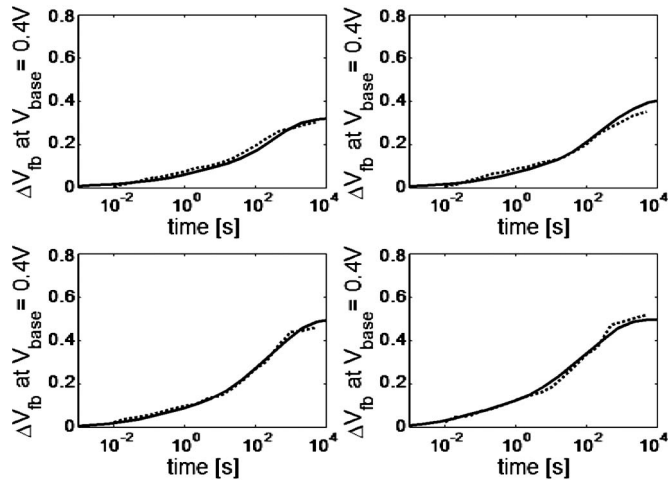


Fig. 13. Fittings of the experimental results obtained with the two-pulse *CV* measurement technique. The dashed lines are the experimental curves, and the solid lines are the simulated curves. Each graph corresponds to a different discharge voltage V_{base} .

to this uniform distribution of defects, does not show any increase in the slope, hence being different as compared to the one predicted by the theoretical results summarized in Figs. 8 and 10. This is due to the fact that, in the experimental case, the traps situated very close to the gate are discharged when the V_{FB} is measured, as explained in Fig. 6. Consequently, the “fingerprint” of these traps, an initial slow V_{FB} variation followed by a slope increase when detrapping toward the substrate starts, will not be seen in the experimental data. The variation of V_{FB} is produced from the beginning by the simultaneous detrapping of charge toward the gate and toward the substrate, resulting in a net slope.

The SiO_2 interfacial layer has been considered trap free in this case. The assumption seems to be reasonable here in view of the well-defined interface observed in the TEM cross sections and composition analysis (not shown). Moreover, the inclusion of traps in the interfacial layer at shallow energies will yield into inflection points in the first part V_{FB} variation curves, which are not observed in the measurements. In the case where the uniform distribution of traps extends slightly into the SiO_2 layer, the V_{FB} variation would be observed earlier, which would yield into a modification of the detrapping constant (or the energy depth of the defects) and a slight decrease of the calculated density of traps.

The second part of the detrapping curve can be reproduced considering as dominated by traps at the interface between the SiO_2 and the high-*k* normally distributed in energy with a central level of 3 eV and a standard deviation of 0.12 eV and at a central level of 3.6 eV with a standard deviation of 0.05 eV. The extracted trap densities are $1 \times 10^{19} \text{ cm}^{-3}$ for the uniform distribution and $3.5 \times 10^{12} \text{ cm}^{-2}$ and $2.3 \times 10^{12} \text{ cm}^{-2}$ for the interfacial distributions, respectively. The obtained fittings for different V_{base} are shown in Fig. 13.

The minimum V_{base} that can be applied is -2 V ; after this value, the fitting slowly loses accuracy, probably due to the high field in the stack that may change the apparent depth of the traps [27], [28]. Indeed, slightly increasing the energy depth of the traps when decreasing V_{base} will allow fitting the measurements

in the whole range of voltages considered because the model overestimates the detrapping speed if the trap depth is kept constant. Furthermore, when decreasing V_{base} , the device enters in a nonsteady deep-depletion state that can bring inaccuracies to the voltage and potential calculations with respect to the time.

A very similar distribution of traps can accurately fit measurements performed in splits with the same fabrication conditions but different Al_2O_3 thickness (not shown), strongly supporting the results obtained.

VII. CONCLUSION

We have demonstrated that the traps in the high-*k* dielectric materials for IPD can be sensed using the two-pulse *CV* technique. The output of this measurement technique, the flatband voltage variation of a charged device during different discharge times and for different discharge voltages, is translated into density and location of the traps in the dielectric by means of a newly developed trapping/detrapping model. The model assumes inelastic trapping and quasi-elastic detrapping of electrons to and from the defects in a dielectric stack. A uniform distribution of defects between 1.4 and 2 eV below the conduction band edge of the high-*k* together with an interfacial distribution of defects between the SiO_2 and the high-*k*, presenting two density peaks at 3 and 3.6 eV, can accurately fit the results obtained with the two-pulse *CV* technique for the considered Al_2O_3 -based dielectric stacks.

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applications.

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