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An assessment of the mobility degradation induced by remote charge scattering

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Carrier mobility reduces when the gate SiON becomes thinner than 2 nm or high-*k* layer is used. Agreement has not yet been reached on the level of reduction and on the underlying mechanism. Remote charge scattering has been proposed to be responsible for the mobility reduction and this work assesses its importance. By increasing charge density at 0.56–1 nm from the substrate interface to the order of 10^{20} cm^{-3}, it is found that both electron and hole mobility changes little. © *2009 American Institute of Physics*. [doi:10.1063/1.3279146]

One driving force for downscaling metal-oxide-semiconductor field effect transistors (MOSFETs) is to improve circuit operation speed. When the gate SiO_2 thickness, T_{ox}, is over 5 nm, carrier mobility is insensitive to T_{ox}.[1] Once T_{ox} is below 2–3 nm, however, mobility reduces for thinner T_{ox}.[2–7] The reported reduction near threshold voltage varies substantially, from a factor over 2 (Ref. 2) to an insignificant level.[4] As gate voltage increases from threshold, the relative mobility reduction can either decrease[2,3] or increase.[4,5] Agreement has not yet been reached on the origin for such phenomenon and the proposed mechanisms include remote charge scattering (RCS) from impurities in depleted poly-Si gate,[2,3,6] increased surface roughness,[4,5] and long-range Coulomb interaction between carriers in the gate and in the inversion layer.[7] Even among the various RCS theories, depending on the assumptions used in the model, the calculated RCS mobility can vary over two orders of magnitude.[2,6]

For the high-k/SiO_2 stack, it has been reported that a reduction in the thickness of interfacial SiO_2 below 2.5 nm can progressively reduce carrier mobility,[3] indicating the presence of remote scattering. Soft optical phonon,[8,9] remote surface scattering,[10] and RCS from charges either in the bulk of high-*k* layer or at the high-k/SiO_2 interface[3,6] can contribute to a lower mobility.

One weakness of early works is that different samples were used when experimentally studying the RCS and this introduces uncertainties. For example, a reduction in T_{ox} cannot only bring the gate closer to the substrate, but could also modulate other factors such as surface roughness.[4,5] In this letter, we will remove these uncertainties and study the impact of RCS on mobility by varying charges in the same device through either processing or electron trapping. It will be shown that RCS has little effect on the effective mobility, when charging reaches a level of 10^{20} cm^{-3} at a location of 0.56–1 nm from the substrate.

The typical doping level for poly-Si gate is $10^{19}-10^{20}$ cm^{-3} and it is proposed that the ionized impurity reduces effective mobility when $T_{ox} \leq 2$ nm.[3,6] As a result, the criteria for selecting test samples are as follows: the dielectric charging can vary in the order of 10^{20} cm^{-3} and must be within 2 nm from the substrate. Four different samples are selected and the details are given in Table I. All samples have a substrate doping of 5×10^{17} cm^{-3}. The channel length is 0.25–0.8 μm and the channel width is 10 μm. The mobility in our sample is similar to that reported by early works[9,11,12] and the net charge in our fresh dielectric stack is insignificant.

The effective mobility is evaluated using the split-CV technique.[1] The electron trapping in the thin dielectric stack is highly unstable[13,14] and mobility can be substantially underestimated if the charge density changes during the I_d-V_g sweep.[15] To suppress this change, I_d-V_g was measured by the fast pulse I-V technique with an edge time of 5 μs.[13,14] The source/drain series resistance[16] and gate leakage[17] was corrected and all measurements were at room temperature.

We will first study the impact of process-induced positive charge (PIPC) on the effective mobility and then assess the effect of electron trapping.

Impact of PIPC on electron mobility: It has been reported that annealing in forming gas (10% H_2) at 500–550 °C can generate positive charging in the HfO_2/SiO_2 stack.[18,19] A typical result for sample A is given in the inset of Fig. 1. Since the detailed spatial distribution of PIPC is not available, its density and separation from the substrate interface must be estimated. On one hand, as a "rule-of-the-thumb" estimation of the farthest possible distance from the substrate, we assume that all PIPC are uniformly distributed in the HfO_2 layer and there is no PIPC in the interfacial SiO_2. The volume density, ρ, can be determined from,[20]

TABLE I. The samples.

Sample	A	B	C	D
Polarity	nMOSFET	pMOSFET	nMOSFET	nMOSFET
T_{Hf} (nm)	2	2	2	1.5
High-*k*: material	HfO_2	HfO_2	HfO_2	HfSiON
Process	ALD	ALD	PVD	ALD
T_{IL} (nm)	0.56	0.73	1	0.77
IL: material	SiO_2	SiON	SiO_2	SiON
EOT (nm)	0.96	1.13	1.62	1.16
Gate material	TaN/TiN	TaN/TiN	TaN/TiN	Poly-Si

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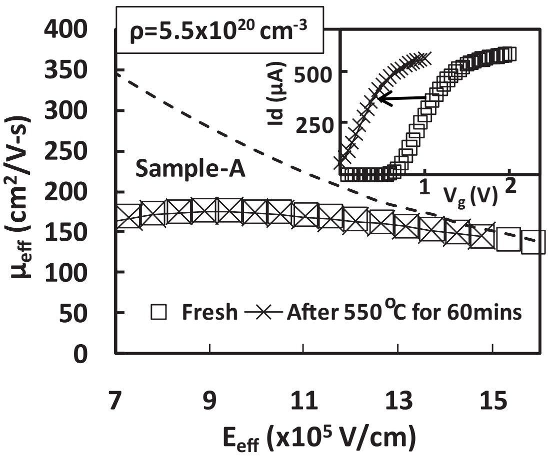

FIG. 1. The effective electron mobility before and after a 60 min exposure to forming gas (10% H_2), leading to a positive charging of 5.5×10^{20} cm^{-3} in HfO_2. The inset shows the I_d-V_g used to calculate mobility and the dashed line is the universal curve.

$$\rho = -\frac{2\varepsilon_o k \Delta V_{th}}{q T_{Hf}^2}, \tag{1}$$

where k and T_{Hf} is the dielectric constant and thickness of high-k layer. A $\Delta V_{th}=0.8$ V from Fig. 1 gives an area density of 1.1×10^{14} cm^{-2} and a $\rho = 5.5 \times 10^{20}$ cm^{-3}, which is in the same order as the typical doping density for a modern poly-Si gate[4,6] and is among the highest charging level observed for MOS devices. On the other hand, as an estimation of the nearest possible distance, we assume that all PIPC are uniformly distributed in the interfacial layer. This gives a $\rho = 5.2 \times 10^{20}$ cm^{-3}, so that the volume density is insensitive to the assumption. We will use the ρ for HfO_2 hereafter.

The effective electron mobility before and after PIPC generation is evaluated and Fig. 1 clearly shows that it changes little through the whole range of effective vertical field. We conclude that the RCS induced by a PIPC of 5.5×10^{20} cm^{-3} at 0.56 nm from the substrate has an insignificant effect on electron mobility.

Impact of PIPC on hole mobility: To test effects of PIPC on hole mobility, sample B is used and the PIPC reached $\rho = 8.2 \times 10^{20}$ cm^{-3} at 0.73 nm away from the substrate interface. Figure 2 shows that hole mobility changes little after the PIPC formation. Similar results were also obtained on a pMOSFET with 1 nm HfSiON (70% Hf) and 1 nm SiON stack (not shown).

Impact of electron trapping on electron mobility: The PIPC originates from hydrogenous species[18,19] and one may assume that its interaction with channel electrons is weaker than the interaction between channel electrons and the ionized impurities in the gate, although there is no experimental evidence for this assumption. To test the sensitivity of RCS to the types of charges, we investigate the impact of electron trapping in the dielectric on electron mobility next.

Although pre-existing electron traps in SiON are negligible,[21] their volume density can reach the order of 10^{20} cm^{-3} in a 4 nm HfO_2 prepared by atomic layer deposition (ALD).[14] The problem is that the electron trapping decreases sharply as the HfO_2 becomes thinner and becomes insignificant for a 2 nm ALD HfO_2.[3,14] We cannot obtain sufficient electron trapping within 2 nm from the substrate interface by using ALD HfO_2, therefore. The RCS influence decays exponentially with distance[4,6] and it is essential to have charges within 2 nm, where RCS was reported to be effective.[2–4] This means that we cannot use ALD HfO_2.

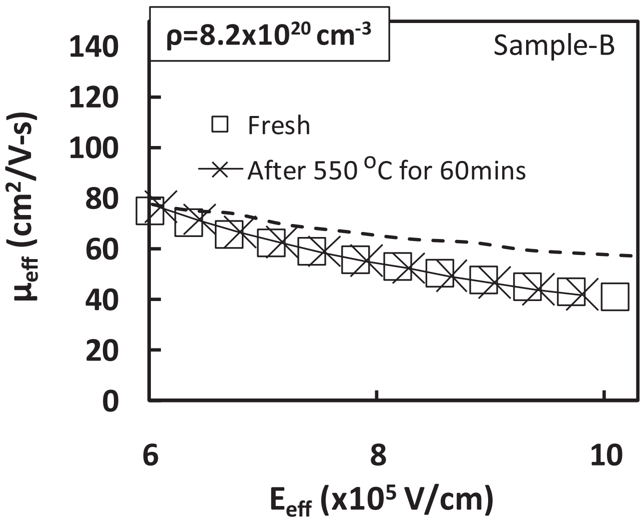

FIG. 2. The effective hole mobility before and after a 60 min exposure to forming gas (10% H_2) that leads to a PIPC of 8.2×10^{20} cm^{-3} in HfO_2. The dashed line is the universal curve.

To overcome the above difficulty, a 2 nm PVD HfO_2 (sample C) is prepared. The inset of Fig. 3 shows that electron trapping leads to a substantial positive shift of I_d-V_g. Since there is little pre-existing electron traps in the interfacial SiO_2,[14,21] we assume a uniform distribution of electron traps in the HfO_2. A $\Delta V_{th}=0.84$ V leads to a volume density of $\rho = 5.8 \times 10^{20}$ cm^{-3}. Figure 3 clearly shows that electron mobility changes little after an electron trapping of $\rho = 5.8 \times 10^{20}$ cm^{-3} at 1 nm from the substrate interface. As a result, changing the type of charges has not changed the conclusion.

Impact of gate material on mobility: The samples used up to here have a TaN/TiN gate and we now test the poly-Si gated sample. PIPC up to $\rho = 2.7 \times 10^{20}$ cm^{-3} were generated at 0.77 nm from the substrate interface. Little change in the effective mobility can be observed in Fig. 4. Our conclusion holds for devices with either metal or poly gate.

To explore why RCS is not as important as previously thought, it is noted that the strength of RCS is sensitive to the assumptions used in the model.[22,23] For example, the inclu-

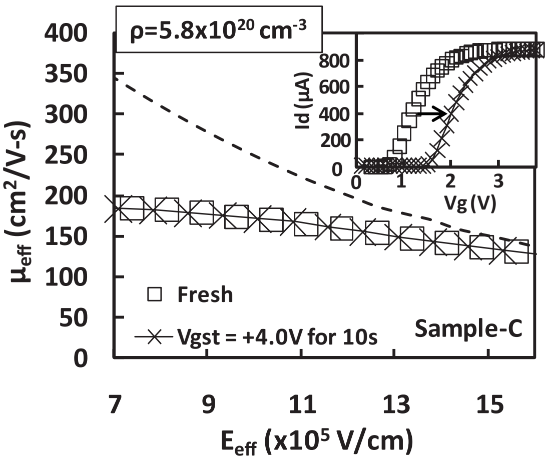

FIG. 3. The effective electron mobility before and after electron trapping of 5.8×10^{20} cm^{-3} in the PVD HfO_2. The inset shows the I_d-V_g used to calculate mobility and the dashed line is the universal curve.

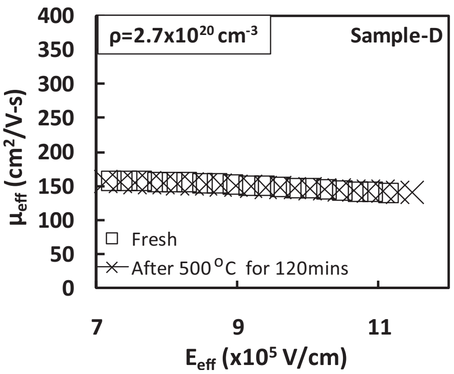

FIG. 4. The effective electron mobility before and after exposure to forming gas (10% H_2) at 500 °C that leads to a PIPC of 2.7×10^{20} cm^{-3}. The dashed line is the universal curve.

sion of gate free carrier screening substantially reduces the effect of RCS on channel mobility[22,23] and it can become negligible when the free carrier density in the gate is sufficiently high.[22]

In conclusion, remote charges of a density in the order of 10^{20} cm^{-3} at 0.56–1 nm from the substrate interface has little effect on the channel mobility, although our results do not rule out that RCS can degrade mobility in principle.

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