On positive charge formed under negative bias temperature stress

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As nitrogen concentration in silicon oxynitride (SiON) increases, negative bias temperature instability (NBTI) becomes a limiting factor for device lifetime. Despite recent efforts, there are confusions and issues remaining unsolved. One of them being how important positive charge formation in SiON is for NBTI and whether all positive charges are the same type. The objective of this work is to investigate positive charge formed in SiON during negative bias temperature stress (NBTS). In comparison with the positive charge formed during substrate hole injection where interface state generation is negligible, it will be shown that NBTS can induce three different types of positive charges: as-grown hole trapping, antineutralization positive charge (ANPC), and cyclic positive charge. Efforts have been made to search for the feature of NBTI, which cannot be explained without involving positive charge. It is unambiguously identified that the impact of measurement temperature on NBTI originates from only one type of defect: ANPC. By using the "on-the-fly" measurement technique, the positive charge density observed in a 2.7 nm SiON can reach to the upper half of 10^{12} cm^{-2}, which is comparable with the positive charge reported for relatively thick SiO_2 (>5 nm). The relative importance of positive charge formation depends on measurement interruption time. The shorter the interruption, the more important positive charge becomes for NBTI. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2427109]

I. INTRODUCTION

Positive charge formation in gate silicon dioxide or oxynitride (SiON) is an important source of device instability.[1–13] It can be formed by irradiation,[1–3] hot carrier stress,[4–6] Fowler-Nordheim tunneling stress,[5,7] hydrogen exposure,[8,9] and negative bias temperature stress (NBTS).[10–19] In comparison with other types of stress, NBTS has received much attention recently.[13–25] This is motivated by the increasing importance of negative bias temperature instability (NBTI) as SiON becomes thinner. A thin SiON requires more nitrogen to block boron penetration and reduce leakage current. It is reported that nitridation enhances NBTI substantially[13–15] and NBTI becomes a limiting factor for the lifetime of *p*-channel metal-oxide-semiconductor field effect transistors (pMOSFETs). Despite recent efforts, there are unsolved issues remaining.

One of the issues is how important positive charge formation in SiON is for NBTI and whether all positive charges are the same type. It used to be accepted that positive charge formation in gate dielectric is equally important as the generation of interface states for NBTI.[11,12,24,25] This verdict has been challenged recently.[20–23] Some researchers believed that interface state generation was dominant during NBTS.[20] Others proposed that the generated interface states alone were responsible for the well-known power law generation kinetics with a power factor of 0.25.[21] It was also suggested that the generated interface states were responsible for the change in device characteristics[22] and only interface state passivation was responsible for the NBTI recovery.[23] This leads to confusion. The objective of this work is to investigate positive charge formation during NBTS.

When positive charge was addressed by recent works on NBTI,[18,19,24,25] all positive charges were considered the same and their properties were not investigated in detail. This work is different from previous ones in three aspects. First, we will show that three different types of positive charges can be generated under NBTS: as-grown hole trapping, antineutralization positive charge (ANPC), and cyclic positive charge (CPC). Second, to demonstrate the importance of positive charge, efforts will be made to search for the feature of NBTI that cannot be explained by the created interface states. It will be shown that the NBTS-induced threshold voltage shift is sensitive to the measurement temperature, but the generated interface states are not. Third, the early NBTI works[11,12,24,25] were typically carried out under a condition where the amount of positive charge is comparable with the interface states. To clearly identify the effect of positive charge, it is desirable to carry out tests under a condition where positive charge dominates. In the present work, this is achieved by stressing the device under substrate hot hole injection (SHI).[26,27] The NBTS-induced positive charge is compared with that formed by SHI and it will be shown that they have the same properties. Finally, to suppress the loss of charge during measurement, the "on-the-fly" technique[19] is employed, which measures the degradation without interrupting stress. It will be shown that the relative importance of positive charge depends on the measurement interruption time.

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II. DEVICES AND EXPERIMENTS

A. Devices

The pMOSFET used for NBTI tests has a surface channel and a $p+$ poly-Si gate. The channel length is 0.15 μm and the channel width is 10 μm. The gate dielectric is a silicon oxynitride (SiON) of 2.7 nm, oxidized at 850 °C, and then nitrided in NO at 1050 °C for 10 s.

The positive charge formed by NBTS will be compared with that created by the SHI technique.[28,29] The pMOSFET used for the SHI has a channel length of 10 μm and a channel width of 200 μm. The gate dielectric is a 5.5 nm SiO_2. Each device has one contact to the n well and one contact to the p substrate, so that the SHI can be carried out.[26,27]

B. Experiments

The stress temperature is in the range of room temperature to 200 °C. The typical gate bias for NBTS is around −3.17 V. The test follows the well-known "stress-then-sense" procedure.[26,27] The NBTS was interrupted at prespecified time to monitor the positive charge and interface states. The measurement takes several seconds, leading to a partial recovery of NBTI. To eliminate this recovery, the proposed on-the-fly technique[19] is also used, where the stress was not interrupted during the measurement. More details on this technique will be given in Sec. III D 1.

The interface state density is measured by using the subthreshold swing technique.[30,31] Positive charge was measured from the gate voltage shift at the midgap point, where the contribution from interface states is negligible.[7,32] The distribution profile of positive charge in the dielectric is unknown. In this work, we follow the well-accepted practice by assuming that the charge centroid is at the dielectric/substrate interface.[26,28,29] The extracted density of positive charge is referred to as the "effective density" of positive charge. The measurement temperature can be either the stress temperature or at some value between the room and stress temperature.

III. RESULTS AND DISCUSSION

A. Typical NBTI generation

Early works[10–12] reported at least three common features for NBTI. First, NBTI originates from two types of defects: generated interface states and positive charge.[10–12] Second, the buildup of NBTI follows a power law against stress time at a given temperature.[11,13,33] Most of the reported power factors are within a narrow range between 0.2 and 0.3. Third, the density of positive charge was found to be approximately the same as the density of created interface states.[11,12,24,25]

Before reporting results and findings, we would like to confirm that the feature mentioned above could also be observed here, so that our test conditions are typical for NBTI and the applied stress voltage is not excessively high.[21] Figure 1 shows that both positive charge and interface states were generated under a gate bias of −3.17 V and a temperature of 100 °C. Their buildup follows the expected power law and a power factor of 0.26 can be extracted by fitting the generated positive charge. The effective density of positive charge, ΔN_{ot} obviously agrees well with the density of generated interface states ΔD_{it}. As a result, the NBTI observed here has all the features reported earlier.

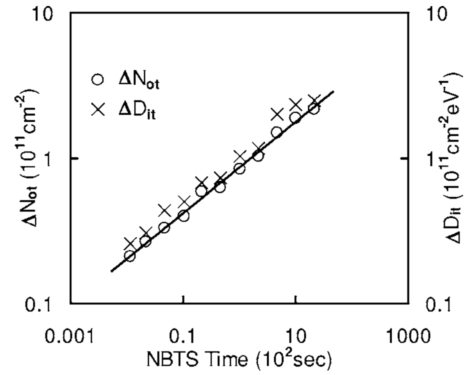

FIG. 1. Buildup of the effective density of positive charge ΔN_{ot} and interface states ΔD_{it} during negative bias temperature stress (NBTS) with a gate bias of −3.17 V at 100 °C. The solid line is obtained by fitting ΔN_{ot} with a power law. The extracted power factor is 0.26.

B. The signature of different defects

The results presented in Fig. 1 do not convince all researchers that positive charge is important for NBTI.[20–23] One may suspect that the so-called positive charge ΔN_{ot} in Fig. 1 is also caused by the generated interface states. Supporting evidence will be given to show that ΔN_{ot} and ΔD_{it} originate from different types of defects.

In Fig. 2(a), the impact of measurement temperature on the threshold voltage shift ΔV_t is given. A device was stressed at 200 °C and then cooled down to room temperature. This is followed by changing the measurement temperature in a sequence of

$$25\ ^\circ\mathrm{C} \rightarrow 65\ ^\circ\mathrm{C} \rightarrow 100\ ^\circ\mathrm{C} \rightarrow 150\ ^\circ\mathrm{C} \rightarrow 200\ ^\circ\mathrm{C} \rightarrow 25\ ^\circ\mathrm{C}.$$

ΔV_t was measured at each temperature and the impact of measurement temperature can be clearly seen from Fig. 2(a). ΔV_t reduces as the measurement temperature rises. To study whether this reduction is caused by the annealing of generated defects, the device was cooled to 25 °C again at the end of the test. Figure 2(a) shows that the ΔV_t returns to its previous level at 25 °C. This confirms that the number of defects is approximately fixed during the above temperature sequence and the observed ΔV_t variation in Fig. 2(a) is caused by changing the measurement temperature.

To explore the origin of this temperature effect, ΔN_{ot} and ΔD_{it} were also measured at each temperature point and the results are plotted in Fig. 2(b). It is obvious that ΔN_{ot} behaves similarly as ΔV_t, but ΔD_{it} is insensitive to measurement temperature. As a result, ΔD_{it} cannot be used for explaining the impact of measurement temperature on ΔV_t and this impact must come from ΔN_{ot}. The different temperature dependences of ΔN_{ot} and ΔD_{it} strongly support that they originate from different defects.

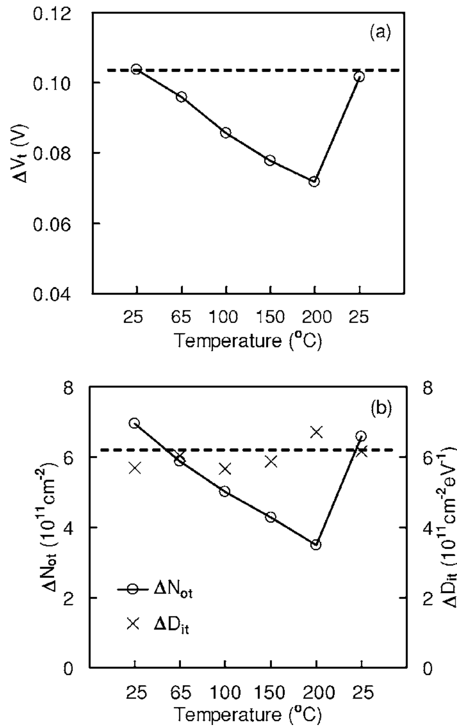

FIG. 2. Impacts of measurement temperature on (a) the ΔV_t and (b) the density of positive charge ΔN_{ot} and interface states ΔD_{it}. A device was stressed at $V_g = -3.17$ V and 200 °C for 200 s. It was then cooled down to 25 °C. This is followed by measurements at different temperatures in the sequence of 25, 65, 100, 150, 200, and 25 °C again. The parameters measured at the start and the end of this sequence at 25 °C are approximately the same. This indicates that the number of defects is approximately the same during this temperature sequence and the variation in ΔV_t and ΔN_{ot} results from changing the measurement temperature. The symbol "×" in (b) shows that the density of generated interface states is insensitive to measurement temperature. The dashed lines are guides for the eyes.

C. Types of positive charge

Although ΔN_{ot} and ΔD_{it} originate from different defects, it does not convincingly rule out that ΔN_{ot} is a different type of interface state. To support that ΔN_{ot} originate from positive charge, we compare its properties with the positive charge formed by a SHI. Unlike the NBTI results given in Fig. 1, Fig. 3(a) shows that the generated interface states are negligible, when compared with the hole trapping induced ΔN_{ot} during the SHI. This makes it a desirable condition for studying the properties of positive charge formed in the gate dielectric.

Our early works[28,29] showed that three different types of positive charge can be formed during the SHI. To facilitate the description and for self-completeness, one typical result in Ref. 28 is reproduced in Fig. 3(b). After SHI, the positive charge was neutralized by an electron injection. Negative and positive gate biases ($|E_{\mathrm{ox}}| = 5$ MV/cm) were then alternately applied with all other terminals grounded. Part of positive charge could be repeatedly charged under $V_g < 0$ and discharged under $V_g > 0$. They are referred to as CPC, as indicated in Fig. 3(b). CPC has similar charging and discharging rates. Figure 3(b) also shows that some positive charges are more difficult to neutralize than their charging and they will be referred to as ANPC. The charging under $V_g < 0$ did not reach the level at the end of SHI, because the

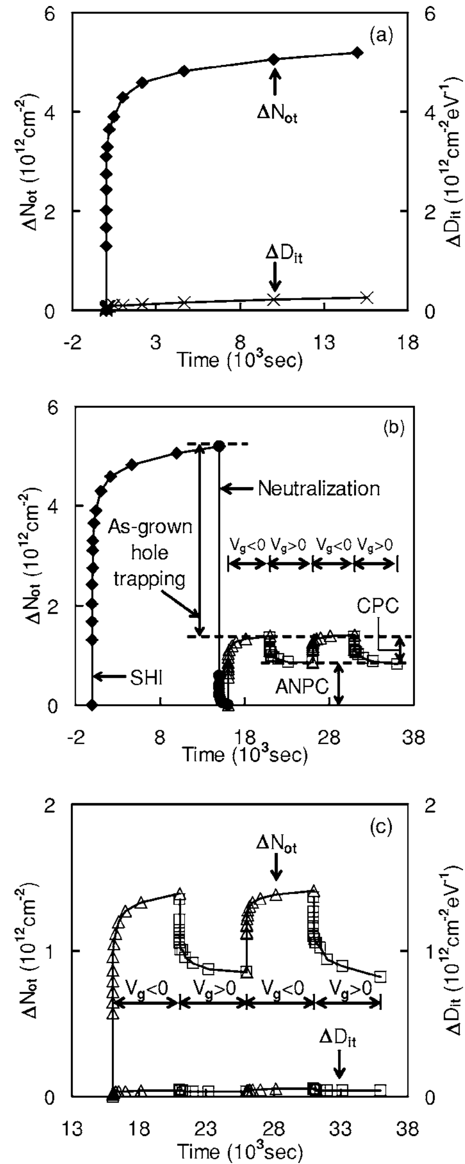

FIG. 3. Positive charge and interface states created during a substrate hole injection (SHI). The SHI was carried out with $E_{\mathrm{ox}} = -5$ MV/cm, an *n*-well bias of 6 V, and a *p*-substrate bias of 7 V on a 5.5 nm oxide. (a) shows that the generated interface states are negligible, when compared with the formed positive charge during SHI. In (b), after SHI, an electron injection was carried out at $E_{\mathrm{ox}} = +8$ MV/cm to neutralize the positive charge. This is followed by applying $V_g < 0$ and $V_g > 0$ ($|E_{\mathrm{ox}}| = 5$ MV/cm) alternately with all other terminals grounded. Three different types of positive charges can be clearly identified: as-grown hole trapping, cyclic positive charge (CPC), and antineutralization positive charge (ANPC) (Ref. 28). (c) shows that the variation of generated interface states after the SHI is negligible.

"as-grown hole traps" cannot be charged without hole injection. To confirm that the ANPC and CPC are not caused by the generated interface states, Fig. 3(c) shows the ΔD_{it} remains negligible when ANPC and CPC were measured after SHI.

To compare the ΔN_{ot} generated by NBTS with the positive charge formed by SHI, negative and positive gate biases ($|E_{\mathrm{ox}}| = 5$ MV/cm) were also alternately applied after NBTS. Figure 4(a) shows that the NBTS-induced ΔN_{ot} has the same feature as the positive charge formed by SHI. In contrast, Fig. 4(b) shows that, after NBTS, ΔD_{it} only exhibits a modest decrease and then remains constant when the gate bias

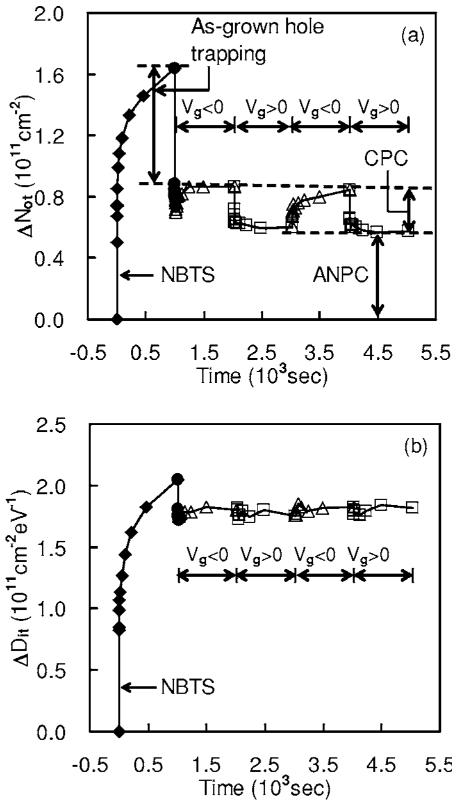

FIG. 4. Positive charge (a) and interface states (b) created by NBTS. The NBTS was carried out at V_g=−3.17 V and 100 °C. It was followed by an electron injection at E_{ox}=+6.5 MV/cm and 100 °C (symbol "●"). Negative (V_g<0) and positive (V_g>0) gate biases ($|E_{ox}|$=5 MV/cm) were then applied alternately, with all other terminals grounded. The similarity between (a) and Fig. 3(b) implies that three types of positive charges were also formed during the NBTS. (b) shows that the generated interface states change little when the gate bias polarity is alternated.

polarity was alternated. This supports that ΔN_{ot} induced by NBTS originates from positive charge, rather than interface states.

The next question is which of the three types of positive charge is responsible for the impact of measurement temperature on ΔV_t and ΔN_{ot} observed in Figs. 2(a) and 2(b). The early work[28] on the SHI-induced positive charge shows that ANPC is the only defect, whose charging reduces with rising temperature. If the ANPC generated by NBTS in Fig. 4(a) is indeed the same as the SHI-created ANPC in Fig. 3(b), one would expect that the charging of NBTS-induced ANPC should also reduce for higher measurement temperature. This is tested below.

After a device was stressed at 200 °C, it was cooled down to 25 °C. The ANPC and CPC were then measured at each temperature point by following the sequence:

$$25\ ^\circ\mathrm{C} \rightarrow 150\ ^\circ\mathrm{C} \rightarrow 100\ ^\circ\mathrm{C} \rightarrow 65\ ^\circ\mathrm{C} \rightarrow 25\ ^\circ\mathrm{C}.$$

Figure 5(a) shows the transient behavior of positive charge when alternating gate bias polarity. Figure 5(b) gives the value of ANPC and CPC as a function of measurement temperature. The results unambiguously confirm that the charging of ANPC generated by NBTS indeed reduces at higher temperature, while the charging of CPC does not. We conclude that ANPC is responsible for the impact of mea-

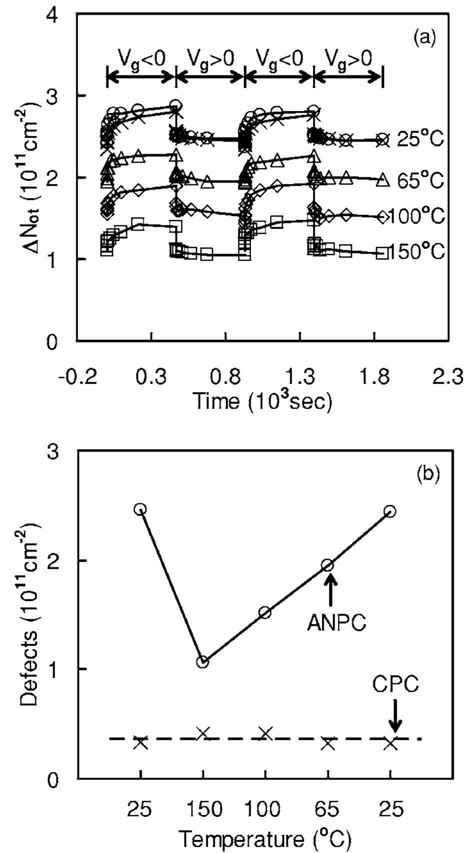

FIG. 5. Effects of measurement temperature on the NBTS-induced ANPC and CPC. A device was first stressed under V_g=−3.17 V at 200 °C (not shown). The ANPC and CPC were then monitored by using the procedure illustrated in Fig. 4(a). The measurement temperature follows a sequence of 25, 150, 100, 65, and 25 °C. (a) shows the transient behavior of positive charge. Symbols "○" and × represent the measured data at the first and second 25 °C, respectively. (b) shows the magnitude of ANPC and CPC at different measurement temperatures.

surement temperature on ΔV_t. The results in Figs. 5(a) and 5(b) strongly support that the same type of positive charge is generated by SHI and NBTS. Consequently, the NBTS-induced ΔN_{ot} also has three components: as-grown hole trapping, ANPC, and CPC.

Figures 6(a) and 6(b) explain why ANPC is more difficult to neutralizing than CPC. The ANPC has energy levels above the bottom edge of the silicon conduction band, but

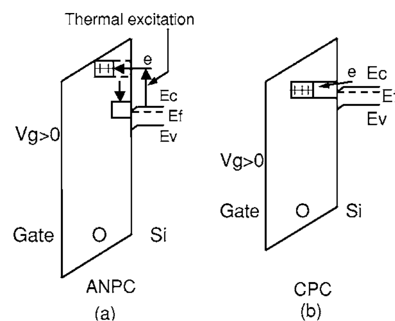

FIG. 6. Energy band diagrams for neutralizing ANPC (a) and CPC (b). The energy level of ANPC is above the bottom edge of silicon conduction band and its neutralization is thermally activated. In contrast, the energy level of CPC is close to the bottom edge of silicon conduction band edge and its neutralization is insensitive to temperature.

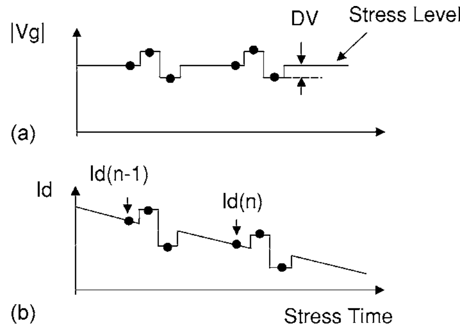

FIG. 7. A schematic illustration of the gate voltage wave-form (a) and the resultant drain current (b) during the on-the-fly measurement. The symbol ● represents the measurement point. DV is the perturbation for assessing the local transconductance. The $I_d(n) - I_d(n-1)$ is the NBTS-induced degradation between two neighboring measurement points.

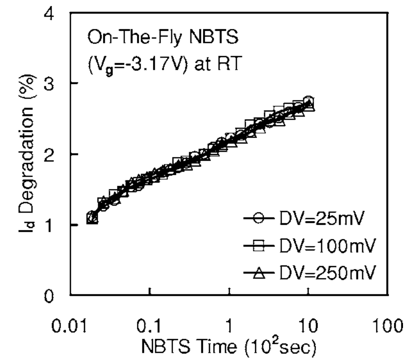

FIG. 8. The degradation of drain current when different gate bias perturbations were used for the on-the-fly measurement. The effect of perturbation is negligible.

the energy level of CPC is closer to this edge. An increase of energy leads to an exponential decrease of the number of electrons in the conduction band of silicon, making the neutralization of ANPC more difficult. Since electron tunneling is a process insensitive to temperature, the neutralization of CPC is insensitive to temperature. However, an increase of temperature raises the number of electron at higher energy levels, which in turn enhances the neutralization of ANPC. This explains why the charging of ANPC reduces at higher temperature.

D. On-the-fly measurements

A comparison of Fig. 3(b) with Fig. 4(a) shows that the NBTI-generated ΔN_{ot} is over one order of magnitude less than the positive charge formed by SHI. The dielectric thickness used is 2.7 nm for NBTI and 5.5 nm for SHI. It is possible that the positive charge in thinner oxide is unstable. The ΔN_{ot} in Fig. 4(a) was measured from the shift of transfer characteristics (TCs) at the midband point and the measurement takes several seconds. The substantial recovery observed for NBTI in early works[34,35] indicates that large losses can occur during the measurement interruption. This loss can lead to a gross underestimation of positive charge formed in the dielectric. It is interesting to find out whether the positive charge in a 2.7 nm SiON can reach a level similar to that shown in Fig. 3(b) ($\sim 5\times 10^{12}\ \mathrm{cm}^{-2}$), if the recovery is eliminated. An estimation can be made by using the on-the-fly measurement.

1. On-the-fly technique

Figure 7 schematically illustrates the voltage wave form used by the on-the-fly technique. The drain current I_d under a stress gate bias V_g was monitored at preset intervals under a drain bias of $V_d = -25$ mV. The ΔV_t was obtained from

$$\Delta V_t \approx -\sum_{n=1}^{N} \frac{I_d(n) - I_d(n-1)}{[g_m(n) + g_m(n-1)]/2}, \tag{1}$$

where $I_d(n) - I_d(n-1)$ is the current reduction caused by NBTS between two successive measurement points, as illustrated in Fig. 7. The $g_m(n)$ is the transconductance at the nth measurement point. To estimate $g_m(n)$, V_g was perturbed by a small amount, ±DV, to give

$$g_m(n) = \frac{I_d(V_g + \mathrm{DV}) - I_d(V_g - \mathrm{DV})}{2\mathrm{DV}}. \tag{2}$$

To ensure that the perturbation of V_g during the measurement has little effect on NBTI, Fig. 8 shows that the degradation of I_d is not affected when DV increases from 25 to 250 mV. DV=25 mV is used in this work and the stress essentially continues during the measurement, so that the recovery is suppressed.

2. Results

Figure 9 shows that the ΔV_t measured by the on-the-fly technique is about one order of magnitude higher than the ΔV_t measured by the traditional TC method. The ΔV_t in Fig. 9 was measured at the stress temperature of 200 °C, while the result in Fig. 3(b) for SHI was measured at room temperature. To eliminate the effects of measurement temperature, the ΔV_t should also be measured at room temperature after NBTS at 200 °C.

In Fig. 10, one device was stressed at 200 °C. It was then cooled down to 25 °C, which took around 4 min, as represented by the dashed line. When measured at 25 °C, ΔV_t is obviously higher than its value at 200 °C, in agree-

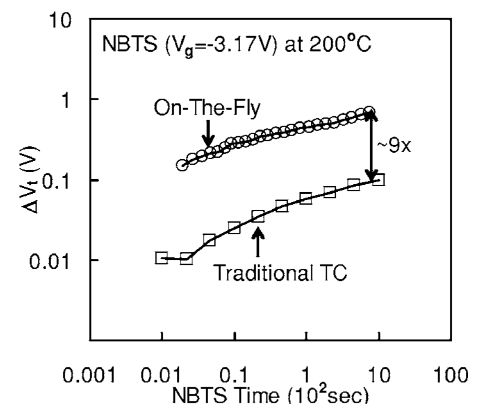

FIG. 9. A comparison of the ΔV_t recorded by the on-the-fly method with that measured from the traditional shift of transfer characteristics (TCs). The former is one order of magnitude higher than the latter. The NBTS was carried out at $V_g = -3.17$ V and 200 °C.

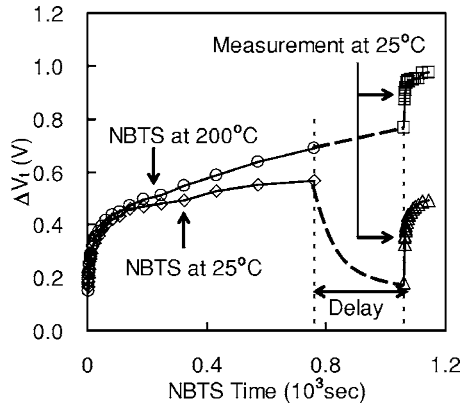

FIG. 10. Effects of measurement temperature on the ΔV_t measured by the on-the-fly technique. A device was first stressed at $V_g = -3.17$ V and 200 °C. It was then cooled down to 25 °C and the ΔV_t was measured again. The ΔV_t at 25 °C is clearly higher than the ΔV_t at 200 °C. When a device was both stressed and measured at 25 °C, a delay between the stress and measurement clearly results in a substantial recovery of ΔV_t.

ment with the observation in Fig. 2(a) based on the traditional TC measurement. Figure 10 also confirms that when the stress and measurement were at the same temperature, a delay between stress and measurement can lead to significant recovery of ΔV_t.

When measured at room temperature by the on-the-fly technique, ΔV_t reaches 0.98 V in Fig. 10, corresponding to an effective charge density of 7.8×10^{12} cm^{-2}. This includes contributions from both the positive charge in the dielectric and the generated interface states. The interface states cannot be directly measured by the on-the-fly method, but we can estimate the up limit of its contribution. For a $(100)\mathrm{Si/SiO_2}$ interface, it is reported that the inherent maximum density of interface states is around 1×10^{12} cm^{-2} eV^{-1}.[36] It is also observed that the interface states generated during electrical stress saturate at approximately 1×10^{12} cm^{-2} eV^{-1}.[37] This means that even if all precursors were converted into interface states, it only accounts for approximately 13% of the observed charge here. When the recovery is eliminated, the positive charge formed during the NBTS can reach to the upper half of the order of 10^{12} cm^{-2}, which is similar to the SHI-induced level observed on a 5.5 nm oxide, as shown in Fig. 3(a).

The results presented in this work show that the relative importance of positive charge in the dielectric for NBTI depends on the measurement interruption time. When the traditional TC with a measurement interruption time of several seconds is used, Fig. 1 shows that the positive charge and generated interface states can be equally important. When the on-the-fly method is used and the recovery is suppressed, positive charge will dominate the ΔV_t.

IV. CONCLUSIONS

In this work, we investigated the positive charge formed in SiON by negative bias temperature stress (NBTS). Unlike previous works on negative bias temperature instability (NBTI), we do not treat all positive charge as a single type of defect. By comparing with the positive charge formed during the substrate hole injection, where the generated interface states are negligible, it is shown that NBTS can create three different types of positive charges: as-grown hole traps, antineutralization positive charge (ANPC), and cyclic positive charge. Attention has been paid to search for the characteristic of NBTI, which cannot be explained without involving positive charge. It is found that, for a given number of defects, the NBTS-induced threshold-voltage shift reduces with increasing measurement temperature. Our results unambiguously show that this temperature effect originates from only one type of defects: ANPC.

To suppress the recovery caused by measurement interruption, the "on-the-fly" technique is used for monitoring NBTI. For a 2.7 nm SiON, the positive charge can reach to the upper half of the order of 10^{12} cm^{-2}. In this case, the NBTI is dominated by the positive charge, since generated interface states should be limited at around 1×10^{12} cm^{-2}, even if all precursors are converted. When measured from the traditional shift of transfer characteristics, the positive charge can be reduced by about one order of magnitude and becomes comparable with the generated interface states. As a result, the relative importance of positive charge depends on the measurement interruption time.

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