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Reliability nano-characterization of thin SiO_2 and $HfSi_xO_y/SiO_2$ gate stacks

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Abstract

In this work, a conductive atomic force microscope (CAFM) has been used in order to detect and electrically characterize the evolution of dielectric degradation on thin (<5nm) SiO_2 oxides and on $SiO_2/HfSi_xO_y$ gate stacks on a nanometer scale. In SiO_2 oxides we illustrate the evolution of the break down event, from the creation of individual leakage spots to their propagation to larger areas of high conductivity. We also report significant changes in apparent topography and current map after stress for both SiO_2 and $HfSi_xO_y/SiO_2$ stacks. Post break down conduction for both dielectrics is modeled and discussed.

Keywords: Conductive atomic force microscope; dielectric breakdown; SiO_2 oxide; $SiO_2/HfSi_xO_y$ gate stack; leakage sites.

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1. Introduction

Most of the research regarding the dielectric reliability of SiO_2 and high k dielectrics on MOS devices is performed by means of standard electrical characterization techniques. These measurements provide spatially averaged information of the dielectric properties over device areas which usually range between 10^{-11}-10^{-8} cm^2. Macroscopical statistical data however suggest that the area in which breakdown (BD) occurs is of the order of 10^{-13}-10^{-12} cm^2 [1], therefore it is probable that the characterization of breakdown on a nanometer scale would provide very valuable information. In order to achieve electrical characterization of the breakdown phenomena on this scale there have been several attempts based on scanning probe microscopies including scanning tunneling microscopy (STM), ballistic electron emission microscopy (BEEM), and scanning capacitance microscopy (SCM). Although STM and BEEM may be more spatially resolved than CAFM, CAFM is being used by the majority of the scientific community due to its simplicity as it does

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not include tunneling of carriers through vacuum. Electrical measurements performed with CAFM can be regarded as simply a nanoscale version of macroscopic electrical measurements with the tip of the AFM being the gate of the “micro” MOS structure. In addition, CAFM does not necessarily require ultra high vacuum conditions and thus it is easy to use for a routine process monitoring.

2. Experimental

In this work we have used an Omicron AFM system in air and in ultra high vacuum (UHV) conditions. The voltage range provided by the Omicron AFM was between -10 V and +10 V and the current measurement range was limited to 3 orders of magnitude ranging from 5 pA to 5 nA. Due to this limited range, currents below the detection limit (5 pA) and above the compliance level (5 nA) could not be recorded. Our CAFM experiments were performed with commercially available Pt/Ir coated tips with a radius of 25 nm. The conductive tips played the role of the metal electrode of an MOS structure. Constant voltage stresses (CVS) were used to electrically stress the samples. To prevent anodic oxidation [2], for all our stressing experiments the tip was grounded while a negative voltage was applied to the substrate of our samples.

The samples under study were (i) device quality 4 nm thermally grown SiO_2 oxides on an n-type Si substrate and (ii) gate stacks comprising of 2nm $HfSi_xO_y$ layer (30%Hf 70%Si) grown by metal organic chemical vapor deposition (MOCVD) on a 1 nm SiO_2 interfacial layer (chemical oxide on p-Si).

3. Results and discussion on SiO_2 oxides.

To begin with, we have investigated the evolution of the BD event for a 4 nm thermally grown SiO_2 oxide. Stressing was performed by means of a Pt/Ir coated tip in UHV. Fig. 1(a) corresponds to a current image taken at V = -0.5 V on a 1 μm x 1 μm portion of the SiO_2 oxide surface. For such a low imaging voltage the current flowing through the oxide was masked by the background electrical noise of our system (5 pA). To electrically stress the oxide, each time the scanning of the whole area (1 μm x 1 μm) was completed, the imaging/stressing bias was increased by -0.5 V and the scan of the same area was repeated. As the stressing progressed and the voltage increased respectively, no change in the current map of Fig. 1(a) was detected for imaging /stressing voltages up to V = -5 V. However, after imaging the oxide area at V = -5.5 V, non homogeneous conduction was observed in the oxides current map as illustrated in Fig. 1(b).

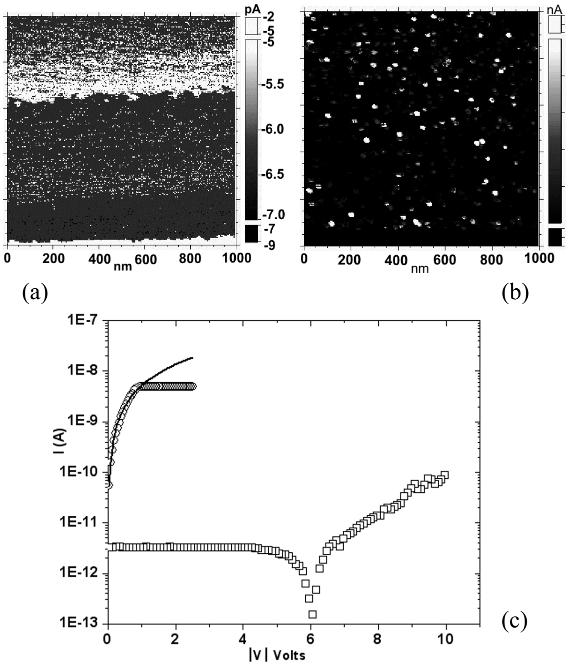

Fig. 1. a) Current map (at a pA scale) of a 4 nm SiO_2 oxide at V = -0.5 V b) Current map (at a nA scale) at V = -5.5 V, where leakage sites begin to appear c) I-V characteristics taken at a BD spot (circles) and at a non broken down region (squares) of Fig. 1(b). Solid line represents fitting to a post BD law. Plateau regions in both IVs are due to the detection limit and compliance of our set up. The “dip” observed at 6V is due to a measurement artifact of the AFM electronics set-up occurring at the onset of current detection ability.

One may clearly observe the creation of leakage sites (white spots), where the current has reached the compliance level of our set up (5 nA). We argue that these locations correspond to individual break down spots. In Fig. 1(c) typical I-V characteristics taken at a leakage site and at the undamaged region of the SiO_2 oxide (black background) are illustrated. The

I-V characteristic of a typical leakage spot has been fitted to a post BD power law:

$$I=aV^b \quad (1)$$

yielding b = 1.37 (i.e very close to linear behavior) which is indicative of a hard break down event (HBD) as demonstrated for example in the work of Miranda and co workers [3] (b=1.8 for 4.2 nm SiO_2).

A key question was whether the SiO_2 breakdown spots were due to the cumulative effect of the multiple scans or only due to the -5.5V stress where the spots begun to appear. The answer is illustrated in Fig. 2(a) where imaging of the stressed area of Fig. 1(b) at a larger scanned area of 5 µm x 5 µm (still at V = -5.5 V) yielded no conduction through the dielectric except in the previously stressed (1 µm x 1 µm) portion of the oxide area. This result indicates that breakdown was due to the cumulative effect of all the previous stresses (from -0.5 V to -5.5 V) rather than the final -5.5 V stress.

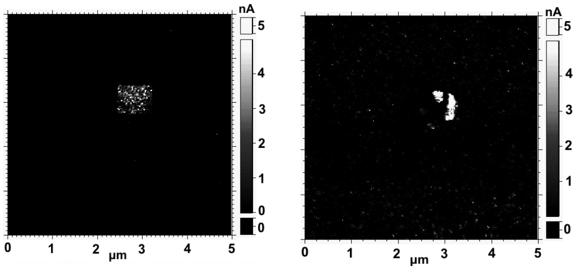

Fig. 2. a) Current map of Fig. 1(b) (at V = -5.5 V) this time imaged at 5 µm x 5 µm. No conduction is observed through the oxide save at the previously stressed area. b) illustration of the BD propagation event. Current image of Fig. 2(a) by increasing the voltage stress at V= -7 V. Individual leakage spots "link" to form larger areas of high conductivity.

To study further the evolution of the BD event, we continued to increase the stressing bias of the 5 µm x 5 µm portion of the oxide area by -0.5 V increments up to V = -7 V. At this higher bias we observed a "propagation" of the BD event as illustrated in Fig. 2(b), that is the individual leakage spots linked together to form large areas of high conductivity. Lateral propagation of the BD event in MOS devices has been previously reported by Lombardo and co workers [4], where it has been demonstrated by means of TEM that the propagation effect was due to the consecutive repetition of breakdown events occurring in close weak (leakage) sites. A macroscopic picture of this phenomenon by means of CAFM has been illustrated in Fig. 2(a) & 2(b) below.

4. Results and discussion on $SiO_2/HfSi_xO_y$ gate stack

Next we discuss the BD event in the case of a $SiO_2/HfSi_xO_y$ gate stack. In order to stress the oxide we have performed consecutive constant voltage scans at V = -10 V on a small portion (50 nm x 50 nm) located in the middle of a much larger 500 nm x 500 nm area. The experiment was performed in air. Results on topography and current map after the stress are illustrated on Figs. 3(a) and 3(b), respectively.

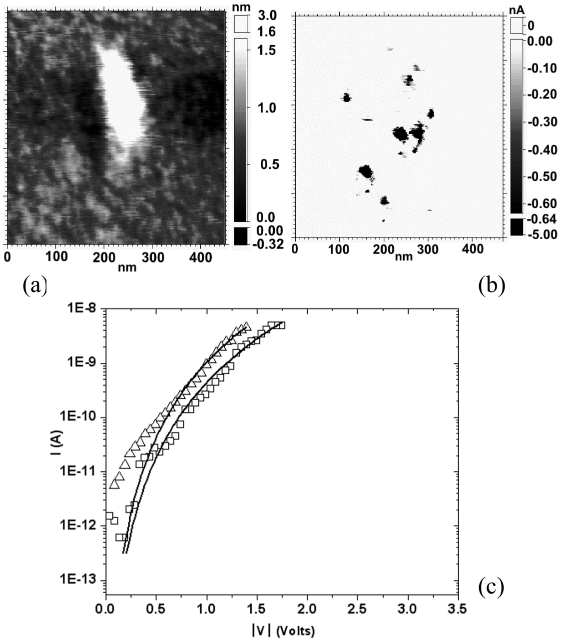

Fig. 3. a) Topographical 'hillock' appearing at the surface of a 2 nm $HfSi_xO_y$/1 nm SiO_2 gate stack after constant voltage stress of V = -10 V. b) Current map of Fig. 3(a) (after stress) at V = -1 V. c) Typical post BD I-V characteristics of the leakage spots illustrated in Fig. 3(b). Solid lines represent fitting of the experimental data to a post BD power law.

From Fig. 3(a) we observe that the constant voltage stress has induced a topographical hillock of 3nm at the vicinity of the oxide surface where the stress took place. Similar topographical features on

SiO_2/HfO_2 gate stacks have been previously reported by others [5] where it has been demonstrated that these changes in topography are not real but artifacts arising from electrostatic interactions between the tip and charge trapped at the BD location. However one cannot exclude the possibility that the observed hillocks represent real topographical damage. Tung et al. for example [6] have observed physical damage after gate oxide breakdown which they have attributed to a dielectric breakdown induced epitaxy model. We believe that in the case of our hafnium silicate gate stacks, structural modifications after stress could be attributed to both charging effects and real structural damage, although further work is needed to substantiate this hypothesis.

Also from Fig. 3(b) it is clear that, as in the case of SiO_2, non-homogeneous conduction is observed at the current map of the gate stack. Typical I-V characteristics at the BD spots are illustrated on Fig. 3(c) where also the experimental post BD I-V curves have been fitted to a post BD power law.

Fitting of the experimental data of Fig. 3(c) to the post BD law of equation (1) yields $a_1 = 1.03 \times 10^{-9}$, $b_1 = 4.58$ (triangles) and $a_2 = 2.47 \times 10^{-9}$, $b_2 = 4.47$ (squares), values which indicate the occurrence of soft break down (SBD). These values are in good agreement with previously reported work in the literature ($a = 8 \times 10^{-9}$, $b = 3.85$) [7] for a 0.6 nm SiO_2/2.5 nm HfO_2 gate stack.

By comparing post breakdown conduction between the 4 nm SiO_2 oxide and the 2 nm $HfSi_xO_y$ /1 nm SiO_2 gate stack, one observes that SiO_2 suffers a HBD event whereas the gate stack suffers from SBD under substrate injection of electrons (tip was always positively biased in respect to the substrate). This result can be explained if one considers that in gate stacks under substrate injection the BD is primarily controlled by the ultra thin 1nm SiO_2 interfacial layer rather than the $HfSi_xO_y$ film [8]. It has been demonstrated [9] that in very thin oxides the transport of electrons is qualitatively different from that in thicker films. In very thin films, the transport is more ballistic than in thicker films and thus the energy which the electrons gain from the electric field is essentially dissipated in the Si substrate and not in the oxide. In effect it is possible that the ultra thin SiO_2 interfacial oxide suffers a less destructive SBD even after a high voltage stress.

5. Conclusions

In summary, in this work we have used a contact conductive AFM in order to study dielectric breakdown at a nanometer scale. In the case of a 4 nm SiO_2 oxide, by gradually applying a constant voltage stress we were able to observe the creation and the subsequent propagation of leakage sites. We have also demonstrated that the creation of the leakage sites was due to the cumulative effect of the gradual stress. By modeling the post break down current through the leakage spots we have concluded that these spots corresponded to HBD events. For the $SiO_2/HfSi_xO_y$ gate stack, the BD leads to a modification in the topography image and to the creation of leakage spots in the current image. Modeling of the post BD conduction revealed that in contrast to thicker SiO_2 films, the gate stack suffered from SBD, a result which was explained by the fact that under substrate injection the BD of the whole stack is controlled by the SiO_2 interface film.

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References

[1] J. Sune, G. Mura, E. Miranda, IEEE Electron Dev. Lett. 21 (2000) 167-169.
[2] D. Hill, S. Sadewasser, X. Aymerich, Proc. SPIE vol. 5118 (2003) 507.
[3] E. Miranda, J. Sune, R. Rodriguez, M. Nafria, F. Martin, X. Aymerich. Jpn J. Appl. Phys. 38 (1999) 2223.
[4] S. Lombardo, A. La Magna, C. Spinella, C. Gerardi, F. Crupi, J. Appl. Phys. 86 (1999) 6382.
[5] X. Blasco, M. Nafria, X. Aymerich, J. Petry, W. Vandervorst, Microelectronics Reliability 45 (2005) 811-814.
[6] C.H. Tung, K.L. Pey, L.J. Tang, M.K. Radhakrishnan, W.H. Lin, F. Palumbo, S. Lombardo, Appl. Phys. Lett. 83 (2003) 2223.
[7] L. Aguilera, M. Porti, M. Nafria, X. Aymerich, Microelectronics Reliability 45 (2005) 1390-1393.
[8] J. Petry, W. Vandervorst, L. Pantisano, R. Degraeve, Microelectronics Reliability 45 (2005) 815-818.
[9] M. Nafria, J. Sune, X. Aymerich, J. Appl. Phys. 73 (1993) 205.