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Microelectronic Engineering 84 (2007) 1951–1955

MICROELECTRONIC ENGINEERING

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Impact of process conditions on interface and high-κ trap density studied by variable T_{charge}-$T_{discharge}$ charge pumping (VT^2CP)

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Abstract

In this paper we use an improved way to measure electrical traps in Hf-based dielectrics by using Variable T_{charge}-$T_{discharge}$ Charge Pumping (VT^2CP). By independently controlling the pulse low and high level timings, we are able to clearly separate the traps in the interfacial SiO_2 from the traps in the High-κ layer, independently of the process conditions and Hf-concentration. The results show that the trap density varies by two orders of magnitude for the samples used in this work, indicating the importance of process optimization.

Keywords: Charge Pumping; Trap Density; Hf-based dielectrics, Plasma Nitridation, Thermal Nitridation, Layer Separation

1. Introduction

In recent years many efforts were made to develop alternative gate dielectrics for future CMOS devices. Hf-based dielectrics are the lead candidate for replacing SiO_2 and SiON. Hf-dielectrics suffer however from a defect band causing V_T-instability [1, 2], reducing mobility [3, 4] and possibly resulting in early breakdown [4]. A thorough understanding of these defects is mandatory for the future integration of these materials in CMOS technologies. However, their characterization is a challenging task, since trapping is highly dynamic in the thin dielectric stack. Recently, we have developed a Variable T_{charge}-$T_{discharge}$ Charge Pumping (VT^2CP) technique, which can potentially separate traps in the interfacial layer (SiO_2) from those in the High-κ layer [5]. The objective of this work is two fold: to further support the layer separation ability of VT^2CP and to investigate the impact of process conditions on trap density in each layer by using VT^2CP.

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doi:10.1016/j.mee.2007.04.048

Table 1.

Process conditions for preparing Hf-based gate dielectric stack. Different thickness, Hf content and Post Deposition Anneal (PDA) were taken in account.'+10s H2O'means that the standard water pulse of 0.3 s in between the ALD cycles was increased to 10 s.

Samples	Interface	High-κ	PDA	MG Degas	EOT (nm)	
1	IMEC clean	2 nm HfO_2	none	std (350, 3m)	1.24	As Deposited
2	IMEC clean	3 nm HfO_2	none	std (350, 3m)	1.45	
3	IMEC clean	2 nm HfO_2 + 10s H_2O	none	std (350, 3m)	1.29	
4	IMEC clean	2 nm HfO_2 + 10s H_2O	none	none	1.67	
5	IMEC clean	2 nm HfO_2	800C-N_2	std (350, 3m)	1.34	RTA
6	IMEC clean	2 nm 80% HfSiO	DPN	std (350, 3m)	1.51	Plasma Nitridation
7	IMEC clean	3 nm 80% HfSiO	DPN	std (350, 3m)	1.46	
8	IMEC clean	4 nm 80% HfSiO	DPN	std (350, 3m)	1.57	
9	IMEC clean	3 nm 50% HfSiO	DPN	std (350, 3m)	1.71	
10	IMEC clean	4 nm 50% HfSiO	DPN	std (350, 3m)	1.94	
11	IMEC clean	3 nm 50% HfSiO	800C-NH_3	std (350, 3m)	1.56	Thermal Nitridation
12	IMEC clean	4 nm 50% HfSiO	800C-NH_3	std (350, 3m)	1.79	

2. Devices and experimental

2.1 Devices

In this paper we characterize fresh SiO_2 / High-κ metal gate stacks. The interface layer was formed by an O_3-based clean of the substrate surface, which resulted in a chemically grown oxide of about 1nm physical thickness ('IMEC clean') followed by an Atomic Layer Deposited (ALD) high-κ layer. Table 1 summarizes the process conditions and thickness of the high-κ gate stacks used in this work. The devices are of n+/ pwell meander-type gate capacitors. The junction and well contacts along the poly-Si stripes are shorted by metal. Because of the junction, a source of carriers is present for inversion mode. The device has 2 poly stripes of 10μm wide and a total area of 10700 μm^2. With these large area structures, the charge pumping current at low frequency can still be resolved.

2.2. Variable T_{charge}-$T_{tdischarge}$ Charge Pumping (VT^2CP)

In 'conventional' CP theory, the measured trap density D_T is interpreted as interface state density, but at low frequencies, near-interface traps can also respond to the gate pulse. In particular, when the high-κ layer is separated from the substrate by a very thin SiO_2 layer, traps in the high-κ layer can be sensed as well [1, 6]. Recently, we have developed a Variable T_{charge}-$T_{discharge}$ Charge Pumping (VT^2CP) technique, which can potentially separate traps in the interfacial layer (SiO_2) from those in the high-κ layer by the independent control of the charging and discharging times [5]. The measurement sequence used in this paper is described in Fig.1: a gate pulse with fixed t_{charge} (=time at top pulse level) and $t_{discharge}$ (=time at base pulse level) is applied for a base level sweeping from inversion to accumulation. Then $t_{discharge}$ is increased while t_{charge} remains unchanged and a new base level sweep is taken.

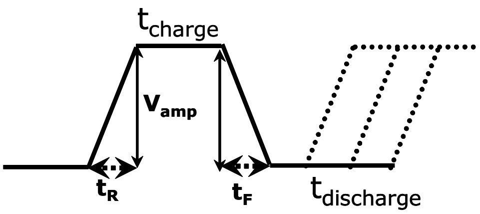

Fig. 1. The pulse applied at the gate with fix t_R, t_F,V_{AMP}, t_{charge}, and variable $t_{discharge}$.

The pulse amplitude V_{AMP} is 1.3V and fall and rise times were chosen sufficiently long to avoid a geometric component for all the samples listed in Table.1. As an example, the base level sweep were done with a fixed t_{charge} = 3μs and $t_{discharge}$ varying from 0.4μs to 5000μs (corresponding to 295 KHz to 200Hz). The results are shown in Fig.2. The discharge time was limited to 5000μs since for longer values the charge pumping current got hidden by the gate leakage current and reliable extraction of D_T was no longer possible.

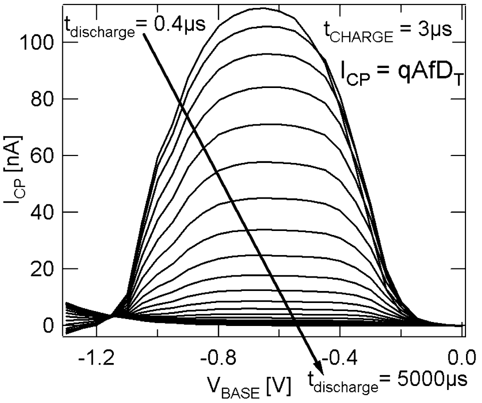

Fig. 2. Typical CP current during VT^{2}CP. As an example the base level was swept with a fixed t_{charge} = 3μs and $t_{discharge}$ varying from 0.4μs to 5000μs (corresponding to 295 KHz to 200Hz). Sample 3 was used.

2.3. *Trap density extraction*

The trap density was extracted using the equation in the inset of Fig.2 with the I_{CP} current monitored at fixed based level. We selected a value as close to zero as possible for each sample (but still in charge pumping regime), to avoid leakage at low frequencies. Fig.3 shows that longer charging (560μs) and discharging time leads to higher trap density, since it allows traps deeper in the dielectric being probed [5].

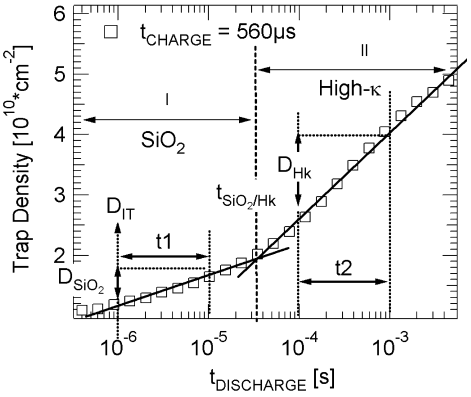

Fig. 3. Separation of traps in interfacial SiO$_2$, (D$_{SiO2}$), regime I, from those in high-κ, (D$_{Hk}$), regime II. Traps per unit area and sensed per decade of $t_{discharge}$ in the SiO$_2$ (D$_{SiO2}$) and high-κ layer (D$_{Hk}$) can be obtained from the slope in the interval t1 and t2 respectively. The trap density D$_{it}$ (at the interface) can be extracted at very short $t_{discharge}$ time (~1μs). Sample 3 was used.

Two regimes can be observed: Regime I and II correspond to the interfacial SiO$_2$ and the high-κ layer, respectively. Traps per unit area and sensed per decade of $t_{discharge}$ in the SiO$_2$ (D$_{SiO2}$) and high-κ layer (D$_{Hk}$) can be obtained from the slope in the interval t1 and t2 respectively. The trap density D$_{it}$ (at the interface) can be extracted at very short $t_{discharge}$ time (~1μs). In the remainder of this work t_{charge} = 560μs is used [5].

2.4. *Support for layer separation*

If the two regimes in Fig.3 indeed originate from two different layers, it may be possible that we can vary the trap density in one layer without affecting the other. Fig.4 shows that 10s water pulse in the ALD process enhances D$_{Hk}$, but has little effect on D$_{SiO2}$. This independent variation of trap density in these two regimes supports that they correspond to two different layers. Note that the trap density in SiO$_2$ is in most cases lower than in high-κ (Fig 3 & 4). This can also be seen from the larger slope in regime II, in comparison with regime I in Figs.3 and 4. In the following, we will use VT^{2}CP to assess the impact of process conditions on the trap density.

3. Results and discussion

3.1. *Impact of nitridation and hafnium concentration*

It is well known that plasma nitridation is superior to thermal nitridation in suppressing Negative Bias Temperature Instability (NBTI) [7].

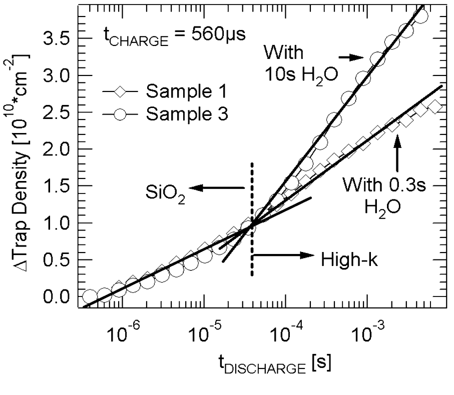

Fig. 4. A long water pulse in the ALD process enhances traps in high-κ layer, but not in interfacial SiO$_2$. This independent variation of trap density in these two regimes (I and II Fig.3) supports that they correspond to two different layers.

It would be interesting to find out how trap density is affected. Fig.5 shows that plasma nitridation used in this work is actually inferior to thermal nitridation for suppressing the trap density, both in the high-κ and in the interfacial layer (SiO_2). We speculate that thermal nitridation leads to a higher nitrogen density towards the substrate interface, which can be responsible for the reduction of the trap density. It has been reported also that HfSiO contains less traps than HfO_2 [8].

This leads to the expectation that a reduction of the Hf-concentration in HfSiO should reduce the trap density. Fig.5 compares two samples with plasma nitrided HfSiO, one with 80% Hf, the other with 50%. It is clear that the sample with the lower Hf concentration actually has a higher trap density. As a result, a reduction of Hf-concentration does not necessarily guarantee a reduction of the trap density.

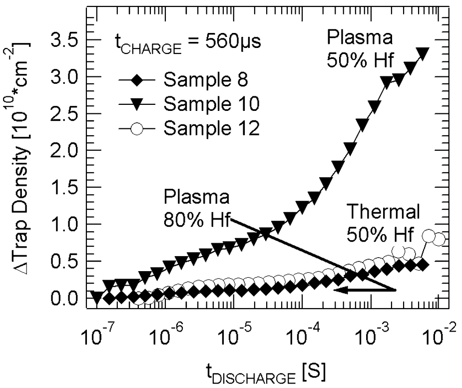

Fig. 5. Impact of nitridation technique and Hf-concentration on traps for 4nm high-κ thickness. Low percentage (50%) of Hf shows higher trap density for plasma nitridation compare to thermal nitridation.

3.2. Degas of metal gate

For the 12 samples listed in Table 1, the lowest trap density was observed in the sample 4, which has a HfO_2 layer, rather than a HfSiO layer. The only process difference between samples 3 and 4 is that sample 3 went through a metal gate degas process and sample 4 did not. The degas was performed at 350°C for 3min. Fig.6 shows that it has a surprisingly large impact on the trap density. Some care is needed in interpreting this result: the significantly higher EOT of sample 4 indicates that the interfacial SiO_2 might have grown as a consequence of the absence of the degas step. This means that high-κ traps will only be sensed at a higher $t_{discharge}$ and the measured low trap density is entirely in the SiO_2. Although trapping is lower without degas, this does not mean that degas should be avoided. Table 1 show that omitting degas leads to an increase of EOT from 1.29 to 1.67nm, which may not be acceptable for commercial application.

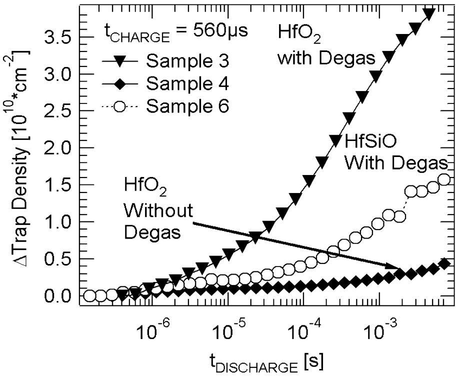

Fig. 6. Impact of metal gate degas on traps. Without degas, trap density in HfO_2 can be lower than that in HfSiO but the EOT increase.

4. Summary

This work supports that the Variable T_{charge}-$T_{discharge}$ Charge Pumping (VT^{2}CP) technique can separate trapping in interfacial layer (SiO_2) from that in high-κ layer by showing that they can vary independently. The water exposure enhances trapping in high-κ layer, but has little effect on trapping in SiO_2. Plasma nitridation can lead to higher trapping in both layers than thermal nitridation. A reduction in Hf concentration does not always reduce trapping.

Figs. 7a & b summarize the impact of process conditions on the trap density in SiO_2 (D_{SiO2}) / high-κ (D_{Hk}) layers and interface states (D_{it}) respectively. In comparison to interface states, trap densities are more sensitive to the process conditions. The trap densities extracted in this work suggest that when using HfO_2, 20% SiO_2 / 80% HfO_2 and 50% SiO_2 / 50% HfO_2, the best process conditions will be as the ones applied to samples 1, 6 and 11 respectively, keeping in mind low EOT. Note that the trap densities variation (2 order of magnitude) of the samples used in this work indicate the importance of process optimization.

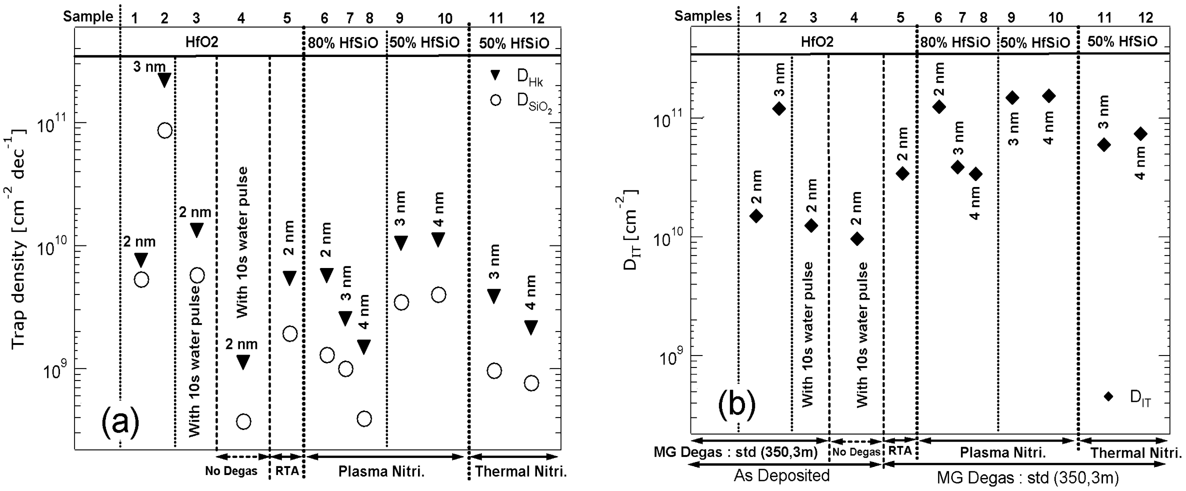

Fig. 7. Summary of the impact of process conditions on trap densities (a) and interface trap density (b). In (a), symbol 'o' and '▼' represent trap density in interfacial SiO_2 (D_{SiO2}) and high-k layer (D_{Hk}), respectively extracted as shown in Fig.3. In (b), interface trap density (D_{IT}) was extracted at $t_{discharge} = 1\,\mu s$.

Acknowledgements

The authors wish to thank the IMEC P-line, the team members of the High k/MG program at IMEC, and the IMEC Core partners (Intel, Samsung, Texas Instruments, Infineon/Qimonda, STMicroelectronics, NXP, Matsushita, TSMC, Micron) for their support.

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