DEFECTS GENERATION IN SiO_2/HfO_2 STUDIED WITH VARIABLE T_{CHARGE}-$T_{DISCHARGE}$ CHARGE PUMPING (VT^2CP).

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ABSTRACT

A Variable T_{charge}-$T_{discharge}$ Charge Pumping (VT^2CP) is used to investigate the creation of traps in the SiO_2 and HfO_2 separately in an ALD SiO_2/HfO_2 metal gate stack. It is shown that by independently controlling the pulse low timing "discharging time" and high level timing "charging time", we are able to separate the traps in the interfacial SiO_2 from the traps in the HfO_2 and observe the creation of new traps in both constituent layers. During degradation the increase of traps, both in the SiO_2 as well as in the HfO_2, follows a power law behavior as a function of time with an exponent ~0.32 and ~0.34 respectively independent of stress voltage. The voltage acceleration of creation of HfO_2 traps (-30) found using VT^2CP is nearly identical of the TDDB (-27) confirming the earlier published model that TDDB occurs when the density of traps in the HfO_2 reaches a critical value. VT^2CP can accurately detect degradation down to a much lower voltage than the dielectric breakdown measurement range and only one stress experiment combined with VT^2CP is sufficient to determine the degradation at a given voltage, while a TDDB test requires many measurements in order to construct an accurate distribution of failure times.

INTRODUCTION

In recent years many efforts were spent on developing alternative gate dielectrics for advanced CMOS devices. In particular, Hf-based dielectrics received considerable attention as possible candidates for replacing SiO_2 and SiON. These dielectrics suffer from a defect band causing Vt-instability [1, 2], reducing mobility [3, 4] and possibly resulting in early BD [4]. Therefore, a thorough characterization of these defects is mandatory for the future integration of these materials in CMOS technologies.

Conventional Charge pumping (CP) technique [5,6] is a very sensitive method to determine substrate/gate dielectric interface state parameters such as the average density D_{it}, the energy distribution within the Si band-gap, the electron and hole capture cross section.

By varying the charge pumping frequency, this technique also allows to characterize bulk defects close to the interface [7], and traps in nitride layers separated from the substrate by a thin SiO_2 layer [8,9]. In some recent papers, charge pumping was used in a similar way for characterizing HfO_2 bulk traps in SiO_2/HfO_2 stacks [1, 10, 11, 12, and 13].

In this paper we further develop the applicability of the variable frequency charge pumping technique by independently controlling the pulse low and high level timings. This allows us to more clearly separate the traps in the interfacial SiO_2 from the traps in the HfO_2 and observe the creation of new traps in both constituent layers.

DEVICES

In this paper we characterize fresh and electrically-stressed thin (EOT = 1.29 nm) Atomic Layer Deposition (ALD) SiO_2 / HfO_2 metal gate stacks. The stack was formed by an O_3-based clean of the substrate surface, which resulted in a chemically grown oxide of about 1nm physical ('IMEC clean'), followed by ALD of 2 nm HfO_2 with 10s of water pulse (H_2O). The devices used consist of n+/ pwell meander-type gate capacitors. The junction and well contacts along the poly-Si stripes are shorted by metal. Because of the junction, a source of carriers is present for inversion mode. The device has 2 poly stripes of 10µm wide and a total area of 10700 µm^2. With these large area structures, the charge pumping current at low frequency can still be resolved.

CHARGE PUMPING (CP)

Conventional Charge Pumping

The basic experimental set-up to perform charge pumping measurements, as introduced by Brugler and Jespers [5] is illustrated in Fig. 1 for the case of an n-channel MOS transistor. The gate of the MOSFET is connected to a pulse generator, which is repeatedly switched from accumulation to inversion and vice versa, while keeping the source, drain and body contacts grounded or slightly reverse biased. During accumulation, some of the majority carriers provided by the body are trapped on interfaces states.

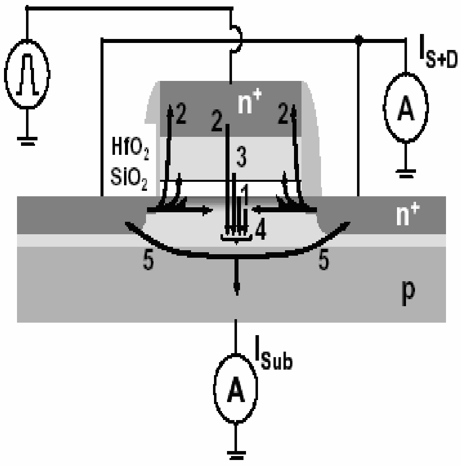

FIGURE.1 POSSIBLE CURRENT CONTRIBUTIONS IN A CHARGE PUMPING MEASUREMENT WITH ALTERNATIVE GATE DIELECTRICS. BESIDE THE RECOMBINATION CURRENT DUE TO INTERFACE STATES (1), THE GATE CURRENT CONTRIBUTION (2), CHARGING AND DISCHARGING OF BULK DEFECTS (3), RECOMBINATION OF INVERSION CARRIERS (4) AND MINORITY CARRIER DIFFUSION (5) DUE TO ELECTRON INJECTION FROM THE HFO_2 LAYER NEED TO BE CONSIDERED.

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During the rising edge of the gate pulse, the mobile majority carriers are collected rapidly from the accumulation layer by the body, and then the trapped majority carriers recombine with the minority carriers provided by the source and drain. Similarly, during the falling edge of the gate pulse, when the gate surface is pulsed from inversion to accumulation, the trapped minority carriers recombine with majority carriers.

This recombination process gives rise to a DC charge pumping current (I_{CP}) in the body, which flows in the opposite direction of the normal drain and source to substrate leakage currents and given by Eq.1

$$I_{CP} = qAfD_T \qquad \text{Eq.1}$$

where q is the electron charge, A the device area, f the frequency and D_T the trap density that can be sensed.

Variable T_{charge}-$T_{discharge}$-Charge Pumping: VT^2CP

In 'conventional' CP theory, D_T is interpreted as interface state density, but at low frequency, near-interface traps can also respond to the gate pulse. In particular, when HfO_2 is separated from the substrate by a very thin SiO_2, traps in the HfO_2 can be sensed [1, 11]. In order to measure these states, a frequency scan is performed with constant duty cycle. When the pulse voltage is high (inversion, Fig. 2), traps are filled through tunneling in both the SiO_2 interface layer and the HfO_2 bulk. We will refer to the time that the pulse is in inversion as the "charging time". When the pulse voltage is low (accumulation, Fig. 2), traps in the interface layer and HfO_2 bulk traps are emptied. We will refer to the time that the pulse is in accumulation as the "discharging time". With a simple frequency sweep at constant duty cycle, both the charging and discharging time of the bulk defects is changed simultaneously. In this work, we will show that an independent control of charging and discharging time allows for an easier interpretation of the data.

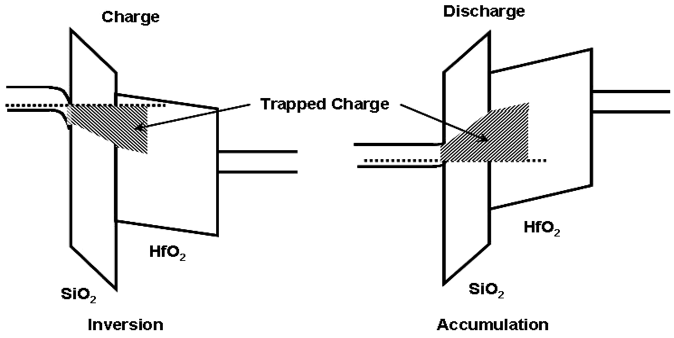

FIGURE.2 SCHEMATIC BAND DIAGRAM SHOWING HOW CHARGING AND DISCHARGING OCCURS WHEN VT^2CP IS USED FOR NMOS.

Note that in conventional CP theory, all the interface states are sensed during the pulse voltage transients *only*. States deeper in the oxide are accessed during the constant high and low voltage parts of the pulse (Figs.2 & 3).

The measurement sequence used in this paper is described in detailed in Figs. 3 and 4: a gate pulse with fixed t_{charge} (=time at top pulse level) and $t_{discharge}$ (=time at base pulse level) is applied for a base level sweeping from -1.3 to 0.2V. Then $t_{discharge}$ is increased while t_{charge} remains unchanged and a new base level sweep is taken.

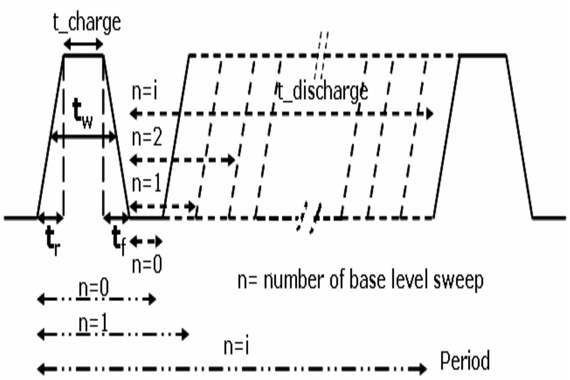

FIGURE. 3 VT^2CP PULSE APPLIED AT THE GATE OF THE DEVICE WITH FIX TR, TF, TW, T_{CHARGE}, AND SWEEPING $T_{DISCHARGE}$.

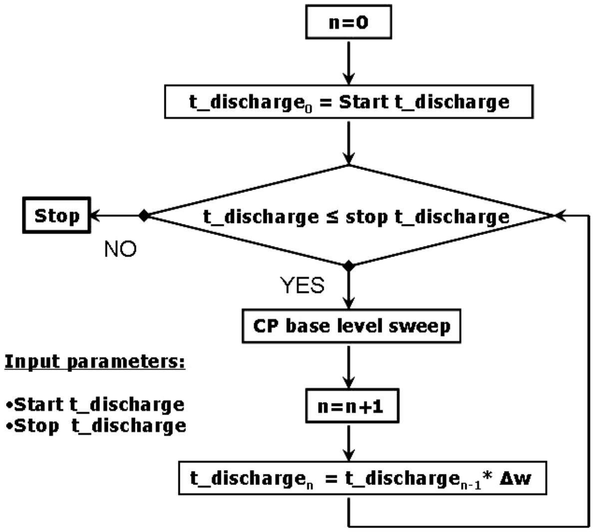

FIGURE. 4 THE MEASUREMENT FLOW DIAGRAM USED TO MONITOR THE ICP CURRENT IN SiO_2 / HfO_2 STACK. ΔW IS THE MULTIPLICATION FACTOR FOR INCREASING $T_{DISCHARGE}$ TIME AFTER EACH LOOP UNTIL STOP T_DISCHARGE IS REACH.

The pulse amplitude V_{AMP} is 1.3V and fall and rise times were chosen sufficiently long (tr = tf = 300 ns) to avoid geometric component. As an example, the base level sweeps was done with a fix t_{charge} = 3μs and $t_{discharge}$ varying from 0.4μs to 5000μs (corresponding to 295 KHz to 200Hz) are shown in Fig.5. The discharge time was limited to 5000 μs since for longer values the charge pumping current was drowned by the gate leakage current and reliable extraction of D_T was no longer possible.

The trap density was extracted using Eq.1 with the Icp current monitored at fixed base level, Vbase = -0.4V. We selected a value as close to zero as possible (but still in charge pumping regime), to avoid leakage at low frequency.

The measurement in Fig. 5 was repeated for different t_{charge} values and the extracted trap densities are summarized in Fig. 6. A schematic drawing of the data in Fig. 6 is shown in Fig. 7.

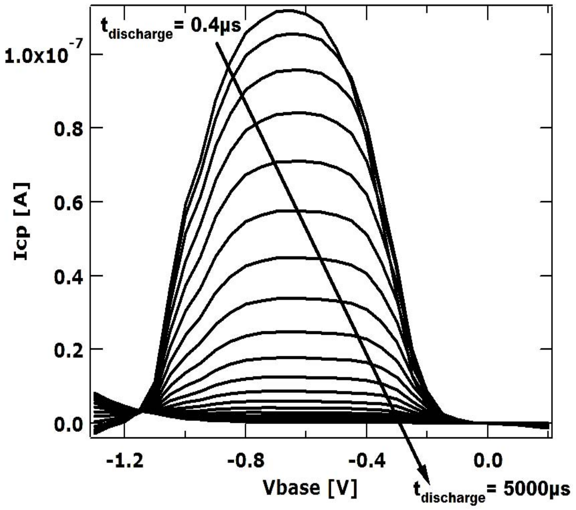

FIGURE.5 CHARGE PUMPING CURRENT VERSUS VBASE USING VT^2CP .VAMP IS 1.3V AND FALL AND RISE TIMES WERE CHOSEN SUFFICIENTLY LONG (TR = TF = 300 NS) TO AVOID GEOMETRIC COMPONENT. EACH BASE LEVEL SWEEP WAS DONE WITH A FIX T_{CHARGE} = 3μS AND $T_{DISCHARGE}$ VARYING FROM 0.4μS TO 5000μS.

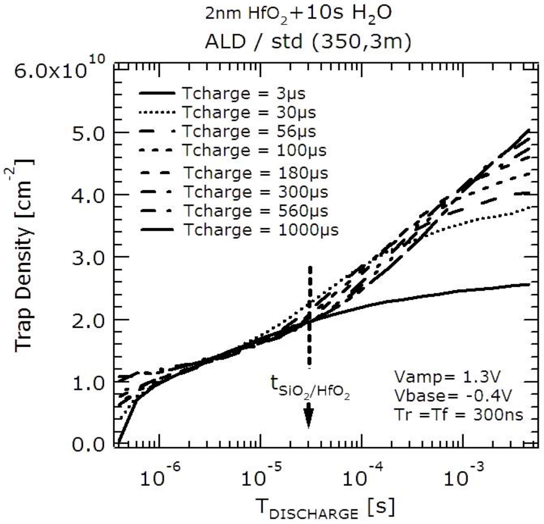

FIGURE. 6 TRAP DENSITY VS. $T_{DISCHARGE}$ AT DIFFERENT T_{CHARGE} FOR 2NM HFO_2 WITH 10S WATER PULSE, USING VT^2CP. THE VERTICAL DOTTED ARROW INDICATE THE $T_{DISCHARGE}$ TIME ($T_{SIO2/HFO2}$) WHEN THE SIO_2/ HFO_2 INTERFACE IS REACHED.

In fig.7 four regimes are indicated that can be interpreted as follows:

I. At the chosen base level (-0.4V in Fig.5), the CP-curve does not reach its full maximum, causing an apparent reduction of the D_T. The drop at short t_{charge} and $t_{discharge}$ is not fully understood at present. In this work, we focus on the result taken at a t_{charge} sufficiently long that this drop is absent.

II. As $t_{discharge}$ increases more traps in the SiO_2 interface layer can respond to the gate pulse. The slope change in the curve at $t_{SiO2/HfO2}$ (=~30-40 μs in Fig. 6) indicates the scanning depth has reached the SiO_2/HfO_2 interface.

III. The bulk states in the HfO_2 are scanned until a saturation level sets in at t_{sat}

IV. No additional traps are measured at longer $t_{discharge}$ time because no charged bulk states are left to be discharged. Note that in Fig. 6 t_{sat} shifts towards longer $t_{discharge}$ as t_{charge} increases.

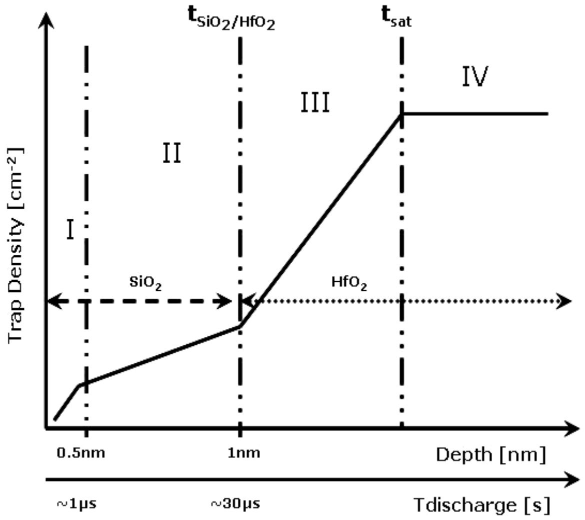

FIGURE.7 USING VT^2CP 4 REGIMES CAN BE INTERPRETED: I) AN APPARENT REDUCTION OF D_T; II) TRAPS IN THE SIO_2 INTERFACE LAYER ARE SCANNED; III) BULK STATES IN THE HFO_2 ARE SCANNED; IV) SATURATION IS REACHED AS NO CHARGED BULK STATES ARE LEFT TO BE DISCHARGED.

There exists disagreement in literature on how deep exactly one can probe in the stack. We interpret the transition between region II and III as the transition between SiO_2 and HfO_2 ($t_{SiO2/HfO2}$ in Fig. 7), but some groups [14] claim that region III is still in the interface layer. We have recently performed an experiment that correlates the SiO_2 thickness with $t_{SiO2/HfO2}$. This correlation provides *experimental* evidence for the interpretation that the traps measured in region III are indeed in the HfO_2, the details of this experiment will be published in a separate paper. Furthermore, if we take the SiO_2 layer to be ~1 nm (from electrical measurement, TEM, XPS*)*, we can show that at $t_{discharge}$=10^{-6} s, the scanning depth is ~0.5 nm (Fig. 7).

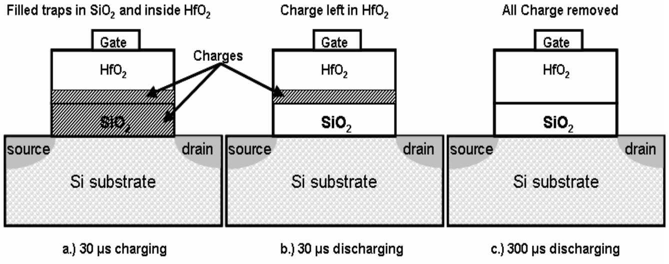

FIGURE.8 SCHEMATIC DRAWING ON HOW TRAPS CAN BE FILLED INSIDE THE HFO_2. A) 30 μS *CHARGE* TIME, CAN FILL TRAPS INSIDE THE HFO_2 ; B) 30 μS *DIS*CHARGE TIME IS INSUFFICIENT TO REMOVE ALL OF THIS CHARGE, ONLY THE SIO_2 LAYER IS DISCHARGED; C) 300 μS DISCHARGE TIME, ALL TRAPPED HFO_2 CHARGE IS ALSO REMOVED.

Note also for ~30 μs *charge* time, we can fill traps inside the HfO_2 as shown in the schematic drawing in Fig. 8a. A 30 μs *dis*charge time ($t_{SiO2/HfO2}$ in Fig.6 & 7) is, however, insufficient to remove all of this charge, since only the SiO_2 layer is discharged (Fig

8b). Only if the discharge time is increased up to 300µs (t_{sat} in Fig. 7), all trapped HfO_2 charge is also removed (Fig. 8c). In other words, the charging mechanism is faster then the discharging mechanism. This can be due to a reduced energy level for a charged state as compared to an uncharged, but also the modification of the oxide field by the trapped charge plays a role.

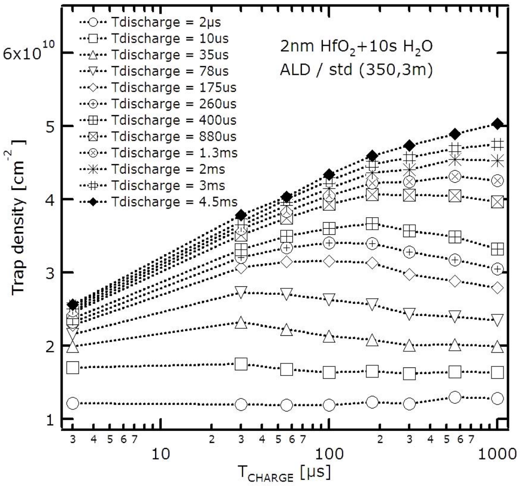

FIGURE.9 TRAP DENSITY VS. T_{CHARGE} AT DIFFERENT $T_{DISCHARGE}$ FOR 2NM HFO_2 WITH 10S WATER PULSE, USING VT^2CP.

Fig. 9 shows the complement of Fig.6: the trap density is plotted versus the charge time for different discharge time. When the discharge time is very short (<30µs) the trap density remain flat, and indicate that we are indeed scanning only the SiO_2 interfacial layer. When the discharge time is higher than 30µs, an increase in the trap density is seen indicating that the traps in the HfO_2 are pumped. For larger charge time a reduction of trap density is observed. Note that the measured trap density reaches a maximum as a function of t_{charge}. This is possibly due to charge redistributed deep in HfO_2 that can no longer be discharged in the applied discharge time; second possible explanation is that the large trapped charge density causes a modification of the internal field.

In the remainder of this work, we fix the charge time at 560 µs in order to avoid region IV as in Fig. 7.

TRAP GENERATION IN SIO_2 AND HFO_2

In this section, we will apply the VT^2CP technique to analyze the generation of traps in a SiO_2/HfO_2 stack under positive Constant Voltage Stress (CVS). In particular, we will investigate the creation of traps in the SiO_2 and HfO_2 separately. The trap density in the interfacial SiO_2, D_{SiO2}, and the HfO_2 trap density, D_{HfO2}, can be determined as shown in Fig. 10. Two linear fits were taken, one in region II (interval t1 in Fig. 10) and one in region III (interval t2 in Fig. 10). The slope in region II (III) gives D_{SiO2} (D_{HfO2}) expressed per area unit and sensed per decade of $t_{discharge}$. Typical values on a fresh device are D_{SiO2}=1.5x10^{10} $cm^{-2}dec^{-1}$ and D_{HfO2}=1.7 x$10^{10}cm^{-2}dec^{-1}$. Note that with the estimated scanning depth as indicated in Fig. 7, the volume trap density in the interface layer is ~$10^{17}cm^{-3}$, in agreement with published data for thicker SiO_2 and SiON layers [16,17]. The volume trap density in the HfO_2 cannot be calculated since the exact scanning depth in the HfO_2 is not known.

In order to measure the trap generation during electrical stress, a Constant Voltage Stress (CVS) is interrupted at regular time intervals and VT^2CP is applied. Note that only one device was used for each CVS combine with VT^2CP measurement.

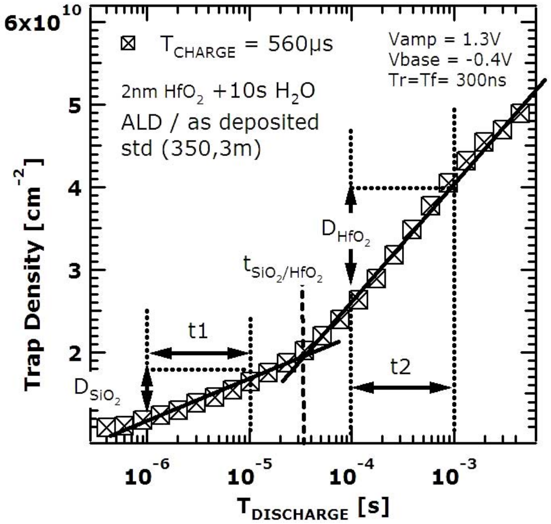

FIGURE.10 THE TRAP DENSITY IN THE INTERFACIAL SIO_2, D_{SIO2}, AND THE HFO_2 TRAP DENSITY, D_{HFO2} DETERMINATION

Fig 11, 12 and 13 shows the time evolution of the trap density versus discharge time at different stress voltages. An increase of the total trap density in both region II and III is observed as summarized in Fig. 14. After subtracting the trap density of the fresh device, the data of both ΔD_{SiO2} and ΔD_{HfO2} can be well fitted by a power law with an exponent of ~0.32 and ~0.34 respectively and independently of stress voltage as shown in Fig. 15.

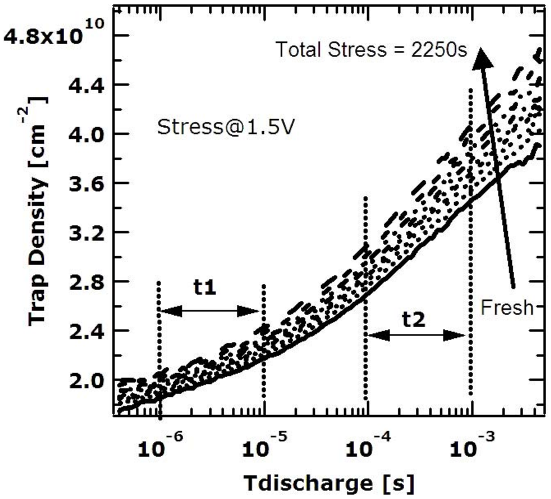

FIGURE.11 TIME EVOLUTION OF THE TRAP DENSITY VERSUS DISCHARGE TIME AT CONSTANT VOLTAGE STRESS = 1.5V, T1 REPRESENT THE INTERVAL FITTED IN REGION II FOR D_{SIO2} AND T2 REPRESENT THE INTERVAL FITTED IN REGION III FOR D_{HFO2}.

Fig. 16 shows the voltage acceleration of the trap generation process for ΔD_{SiO2} and ΔD_{HfO2} (derived from Fig. 15). A power law voltage acceleration is used and we find voltage acceleration exponent of -34 and -30 respectively. TDDB-measurements, also plotted in Fig. 16, show a voltage acceleration exponent of -27, nearly identical to the D_{HfO2} acceleration exponent. This is consistent with the model that dielectric breakdown occurs when the trap density in the HfO_2 reaches a critical value [12, 13].

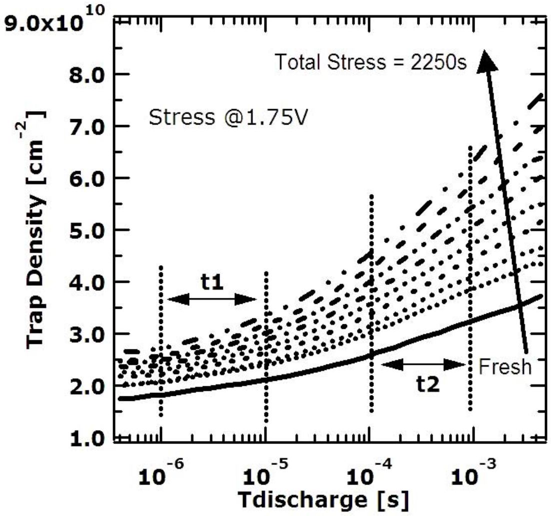

FIGURE.12 TIME EVOLUTION OF THE TRAP DENSITY VERSUS DISCHARGE TIME AT CONSTANT VOLTAGE STRESS = 1.75V, T1 REPRESENT THE INTERVAL FITTED IN REGION II FOR D_{SIO2} AND T2 REPRESENT THE INTERVAL FITTED IN REGION III FOR D_{HFO2}.

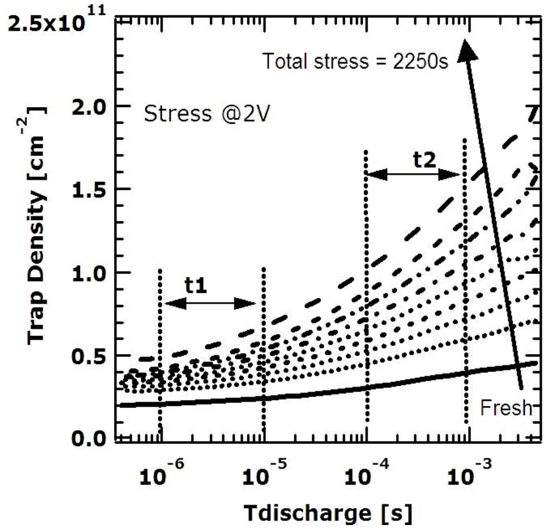

FIGURE.13 TIME EVOLUTION OF THE TRAP DENSITY VERSUS DISCHARGE TIME AT CONSTANT VOLTAGE STRESS = 2 V, T1 REPRESENT THE INTERVAL FITTED IN REGION II FOR D_{SIO2} AND T2 REPRESENT THE INTERVAL FITTED IN REGION III FOR D_{HFO2}.

Note that the VT^{2}CP can accurately detect degradation down to a much lower voltage than the dielectric breakdown measurement range. Furthermore, only one stress experiment combined with VT^{2}CP is sufficient to determine the degradation at a given voltage, while a TDDB test requires many measurements in order to construct an accurate distribution of failure times.

Note also that the agreement between high voltage TDDB and low voltage VT^{2}CP data is only obtained if a *power law* voltage acceleration is assumed and not if an exponential model is taken (Fig.16). The data therefore confirm that power law [13, 15] describes the voltage acceleration of dielectric degradation more consistently than exponential models.

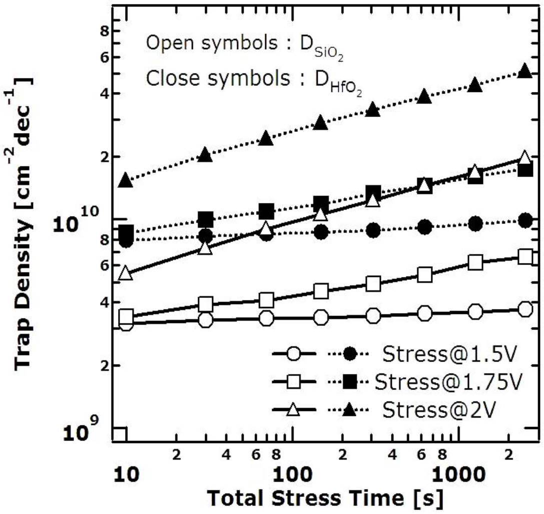

FIGURE.14 TOTAL TRAP DENSITY SENSED PER DECADE FREQUENCY DURING STRESS IN BOTH REGION II (D_{SIO2}) AND III (D_{HFO2}) AT 1.5V, 1.75VAND 2 V.

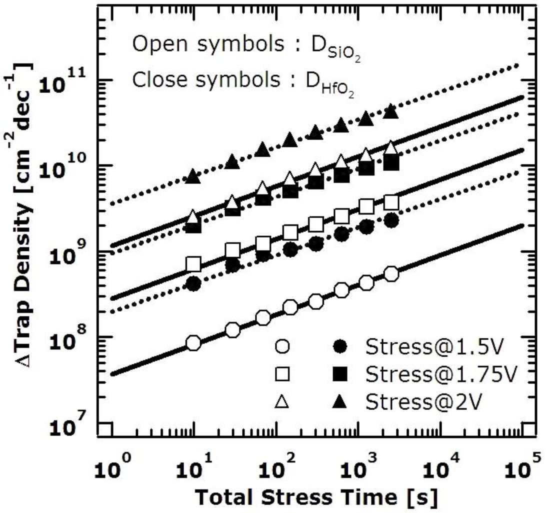

FIGURE.15 ΔT_D VS. TOTAL STRESS TIME SENSED PER DECADE FREQUENCY DURING STRESS IN BOTH REGION II (D_{SIO2}) AND III (D_{HFO2}) AT 1.5V, 1.75V, AND 2 V. DATA CAN BE WELL FITTED BY A POWER LAW WITH AN EXPONENT OF ~0.34(D_{HFO2}) AND ~0.32(D_{HFO2}), INDEPENDENTLY OF STRESS VOLTAGE.

CONCLUSIONS

We discussed an improved way to measure electrical traps and trap creation in SiO_2/HfO_2 stacks by charge pumping. By independently controlling the pulse low and high level timings, we are able to clearly separate the traps in the interfacial SiO_2 from the traps in the HfO_2 and observe the creation of new traps in both constituent layers. We found that the trapping mechanism is faster than the detrapping mechanism.

During degradation at a constant positive voltage, the increase of traps, both in the SiO_2 as well as in the HfO_2, follows a power law behavior as a function of time with an exponent ~0.32-0.34. The voltage acceleration of creation of HfO_2 traps matches that of the TDDB. This confirms the earlier published model that TDDB occurs when the density of traps in the HfO_2 reaches a critical value.

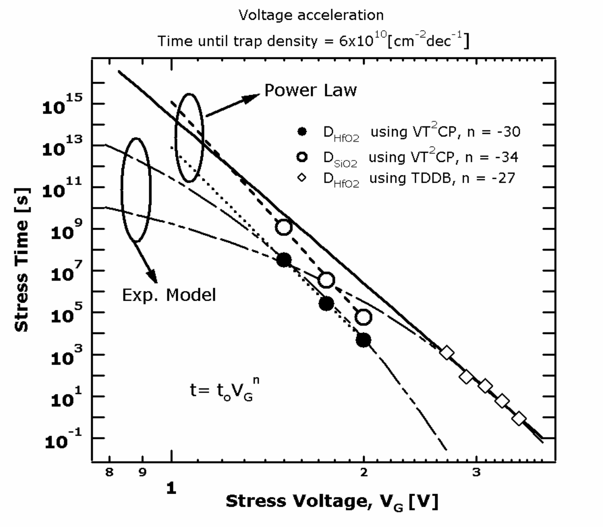

FIGURE.16 VOLTAGE ACCELERATION OF THE TRAP GENERATION PROCESS AT A FIX TRAP DENSITY FOR D_{SIO2} AND D_{HFO2} USING VT^2CP AND TDDB. A POWER LAW VOLTAGE ACCELERATION OF -34 FOR D_{SIO2} AND -30 FOR D_{HFO2} IS FOUND WHEN VT^2CP IS USED, WHICH IS NEARLY IDENTICAL TO THE D_{HFO2} ACCELERATION EXPONENT FOUND WITH TDDB-MEASUREMENTS.

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