

Advanced electrical characterization toward (sub) 1nm EOT HfSiON – hole trapping in PFET and L-dependent effects

^{1,2}M.B.Zahid, ¹L.Pantisano, ¹R.Degraeve, ^{1,4}M.Aoulaiche, ^{1,4}L.Trojman, ^{1,4}I.Ferain, ³E. San Andrés
^{1,4}G.Groeseneken, ²J.F. Zhang, ^{1,4}M.Heyns, ¹M.Jurczak, ^{1,5}S. De Gendt

¹IMEC, ²JMU Liverpool, ³UCM Madrid, also KUL ⁴ESAT and ⁵Chemistry dept.

Introduction

Hf-based gate dielectrics layers with EOT<1nm are actively investigated for 22nm node and beyond. EOT scalability of these films is simultaneously achieved by reducing the high-k thickness as well as optimizing the N-profile into the thin film. For Hf-based layers electron traps in the upper part of the bandgap have been a major concern for nMOSFETs since they cause V_T -instability and affect mobility [1]. With the scaling of EOT to 1 nm and below, the impact of these traps has, however, disappeared [2]. Electron traps have never been considered a potential problem for PMOS because at negative bias they are always efficiently discharged.

We found, however, that in PMOS with EOT ~1 nm, a large hysteresis at high field is observed in the I_D - V_G characteristics, while no hysteresis is measured on the corresponding NMOS devices (on the same wafer) (Fig. 1).

In this work we will prove by an *advanced charge pumping technique* that the *hysteresis in PMOS is caused by hole traps* in the high-k layer. Furthermore, we show how *NBTI defects are correlated with such hole traps*. Hole trap density depends on the Hf- and N-profile in the film, being larger for Hf-rich films.

Experimental devices

Several Hf-based PMOSFETs with HfSiO gate dielectric were manufactured. EOT is ranging from 1nm to 1.8nm (Table 1). Up to 19% Nitrogen was incorporated in the films by either thermal or Decoupled Plasma Nitridation (DPN). PVD TaN or ALD TiN gates were used. Both N- and PMOS were fabricated on the same wafer / Metal Gate (MG) process. Junction activation temperatures in excess of 1000 °C were considered.

Hole trapping in pMOS

In principle, the hysteresis in Fig.1 can be explained in two possible ways (Fig. 2): **a**) electrons traps in the upper part of the high-k bandgap are discharged at large $V_G < 0$; **b**) holes are trapped and detrapped in the bottom part of the high-k bandgap.

Charge Pumping (CP) can distinguish between the two mechanisms, since it only senses holes that are pumped from the source/drain to the substrate, while electrons that are both discharged and charged to the substrate are not measured. In order to access traps in the high-k, low frequencies need to be used and for ~1 nm EOT layers gate-to-substrate leakage current is masking the charge pumping current (Fig. 3). We developed a methodology to separate the charge pumping signal from the leakage current. This method exploits the property that $I_{SUB} = I_{SD}$ if leakage components are absent. Details on this method will be published elsewhere. With this in mind the same pulse as the one in the inset of Fig.1 was considered.

After leakage current correction, the hole trap density is obtained as a function of trap discharge time using the VT²CP method [3] (Fig. 4). The slope of the curve for long discharge time is a measure for the high-k hole trap density. In all the investigated samples the I_D - V_G hysteresis can be explained by

the hole trap density measured by VT²CP proving that mechanism b) in Fig. 2 is correct.

Impact of Nitridation on hole trapping

We studied the impact of different nitridation processes (Table 1) on the hole trap density. Table 1 summarizes the findings for all dielectrics and MG considered. Incorporating N introduces hole traps, both for DPN and NH₃ nitridation. For TiN the largest Hf concentration gives a higher hole trapping. For a given TaN, especially for a high energy DPN process (Hard DPN) the trap density increases drastically suggesting a structural change in the high-k as shown in Fig 4 and Table 1. The hole trap density also affects the NBTI characterization. At low stress field the samples with high hole trap density (Hard DPN) also show a larger NBTI degradation (Fig. 5), that cannot be explained by interface trap generation [4]. Consequently, the extrapolated NBTI lifetime (not shown) follows the same trend as the hole trap density. Importantly all samples still meet the 10 years reliability target.

Several hole trap generation mechanisms can be proposed to explain the data in table 1. However from Fig. 4 these defects are found **a**) in the bulk HfSiON and (see table 1) **b**) preferentially for high-Hf concentrations.

L-dependent hole trapping - a change in the dielectric?

When the L-dependencies of the linear V_T is considered for 1nm and 2nm Hf-rich HfSiON a large roll-off is found for the thicker sample (see Fig.6a). This roll-off is commonly interpreted as lateral nonuniformity (see the model of Fig.6b) associated with processing (etching, a change in the interfacial oxide thickness and quality, lateral diffusion of impurities ...). Note that an effective *negative* charge incorporation in the order of 10¹²/cm² may well explain the results of Fig.6a. Additionally to such a negative charge, also a L-dependent hole trap densities are found using charge pumping, as shown in Fig.7 and 8. Note that the L-dependent increase in the CP signal cannot be attributed to a thinning of the interfacial layer or a change in its dielectric properties, as demonstrated using a split RFCV [5] (Fig.9) and mobility extraction for sub-100nm MOSFETs [6] (Fig.10).

All these characterization techniques point toward a process-induced L-dependent modification of the bulk HfSiON defects. Tentatively phase separation in HfSiON and consequent formation of SiO_x species in the dielectric can explain the large hole trapping.

Summary and conclusions

Unexpected V_T -instability in PMOS was demonstrated for HfSiON with EOT ~1nm. These traps were successfully identified as hole traps in the HfSiON bulk using a modified "leakage-free" CP technique. Hole trap density depends on the Hf- and N-profile in the film and significantly lowers the NBTI lifetime. Largest hole trap densities were found in thin Hf-rich films thus being a concern for further EOT scaling toward sub 1nm EOT. Additionally L-dependent hole trapping was found correlated with traps responsible of anomalous V_T -roll-off.

Acknowledgments: IMEC IIAP on high-k/MG and Emerald

References:

- [1] M. Houssa *et al.*, Mat Science Eng 51 2006; [2] M. Quevedo-Lopez VLSI 2006; [3] M.B. Zahid, to be presented IRPS 2007; [4] Aoulaiche IRPS 2006; [5] E. San Andres, EDL 2006; [6] E. San Andres submitted INFOS 2007; [7] S. Severi, EDL 2006.

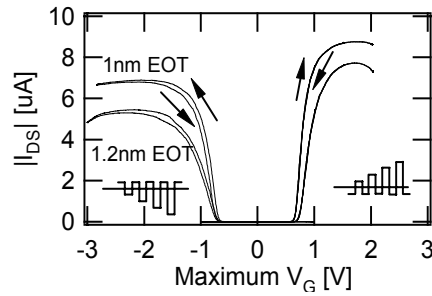


Fig.1: 1 nm EOT PMOS show large hysteresis while nothing is observed for NMOS (note the same wafer / die for both NMOS and PMOS).

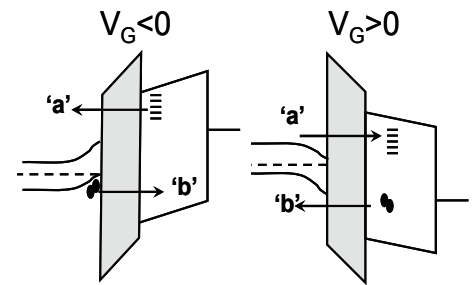


Fig.2: Charging and discharging of defects during CP. Electron traps in the upper part of bandgap (a) and hole traps in the lower part (b).

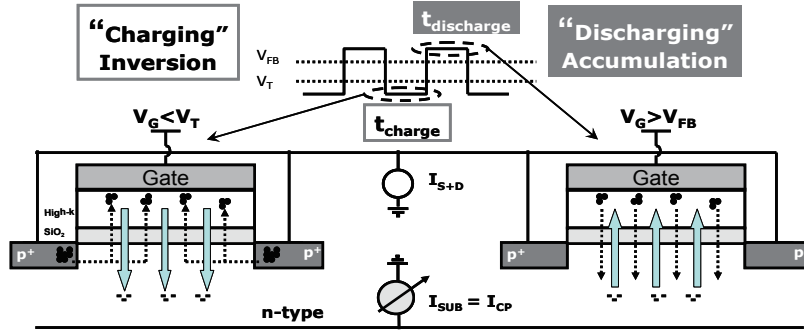


Fig. 3: During charge pumping a gate pulse toggles the MOSFET from inversion to accumulation. Holes from the source/drain are trapped in the dielectric during inversion and released during accumulation. For $J_{gate}=0$, $I_{sub}=-I_{SD}=I_{CP}$. For large J_{gate} a correction is needed in the low frequency range by using conventional I_G-V_G measurements on the same samples.

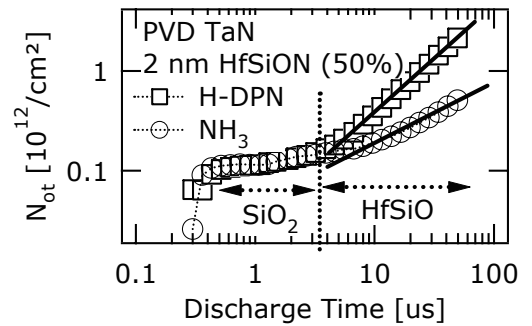


Fig.4: Hole traps density as a function of trap discharge time (defined in Fig. 3). On this plot we can separate the traps in the interface from those in the high-k (VT²CP method [3]). The slope of the curve in the long discharge time region is a measure for the high-k trap density.

HfSiON Thickness	Hard DPN	Soft DPN	NH ₃	N ₂	Hf [%]	ΔV_T [mV]	N_{ot} [cm ⁻²]	EOT [nm]	
2 nm					50	5	5.7E+10	1.80	PVD TaN
2 nm					50	7	9.5E+10	1.67	
2 nm					50	22	3.0E+11	1.58	
3 nm					50	32	3.9E+11	1.78	
2 nm					50	40	5.3E+11	1.62	
2 nm					50	44	7.6E+11	1.25	ALD TiN
2 nm					80	52	8.6E+11	1.30	
1 nm					80	44	9.5E+11	1.05	

Table 1: Table showing the different sample used in this work as a function of several important parameters. The V_T shift was taken at $I_{dmax}/2$ from the ramp-up and -down of the pulsed I_D-V_G curve in all case. Note that the **worst case condition is for Hf-rich samples**.

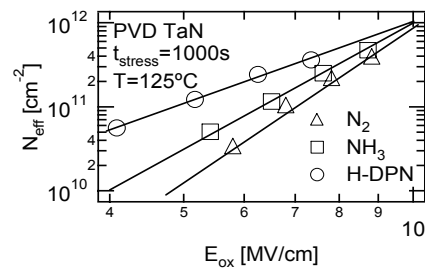


Fig.5: The effective charge density after 1000s NBTI stress vs. the stress field. Samples with high hole trap density show a large degradation at low field.

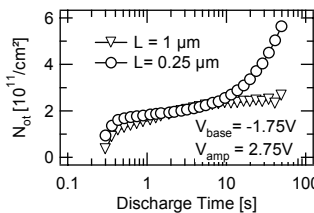
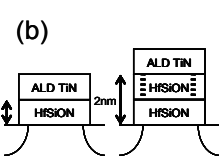
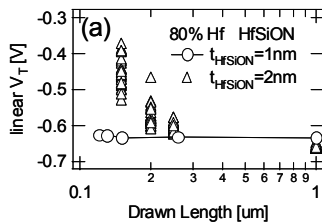


Fig.6: a) Lateral non uniformity (LNU) causes a dramatic V_T -roll off for both PMOS and NMOS (not shown); b) Model of electrical data. Note the defects responsible of LNU in 2nm HfSiON.

Fig.7: Hole trapping increases dramatically with shorter L, consistent with Fig.6b

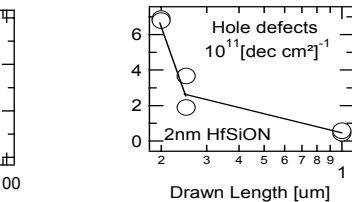


Fig.8: Hole defects in HfSiON vs. gate length. Note that the hole trap densities found are in the same order of magnitude of the electron defects responsible of V_T -roll off in Fig.6a

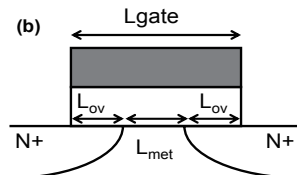
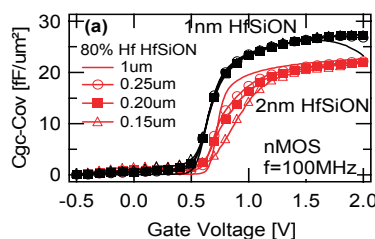


Fig.9: a) Normalized split RFCV [5] for 1nm and 2nm HfSiON with nominal gate length down to 0.15um. **Despite the distortion close to V_T (LNU), for 2nm HfSiON the CET is L-independent.** b) The RFCV were normalized [6] taking into account the L_{gate} (measured with CDSEM) and the overlapping length L_{ov} (as in [7]). Once L_{ov} is known for the 'ideal' 1nm HfSiON case, its value can be also used to normalize the 2nm HfSiON for all gate lengths.

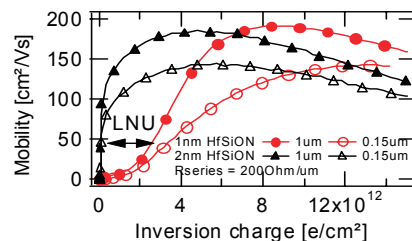


Fig.10: Mobility for 1um and 0.15um. Extraction technique discussed in [6]. The charge in inversion and L_{met} has been determined from Fig.9. $R_{series} = 200\Omega/\mu m$ for both samples. A **L-independent peak mobility is found for both dielectrics suggesting a negligible change in the interfacial oxide quality.** (the lateral nonuniformity (LNU) already discussed in Fig.9 yields a slight perturbation in the inversion charge calculation without affecting the overall conclusions)