

Dominant Layer for Stress-Induced Positive Charges in Hf-Based Gate Stacks

Jian F. Zhang, Mo Huai Chang, Zhigang Ji, Lin Lin, Isabelle Ferain, Guido Groeseneken, Luigi Pantisano, Stefan De Gendt, and Marc M. Heyns

Abstract—Positive charges in Hf-based gate stacks play an important role in the negative bias temperature instability of pMOSFETs, and their suppression is a pressing issue. The location of positive charges is not clear, and central to this letter is determining which layer of the stack dominates positive charging. The results clearly show that positive charges are dominated by the interfacial layer (IL) and that they do not pile up at the HfSiON/IL interface. The results support the assumption that positive charges are located close to the IL/substrate interface. Unlike electron trapping that reduces rapidly for thinner Hf dielectric layer, positive charges cannot be reduced by using a thinner HfSiON film.

Index Terms—Hf silicates, high- k gate dielectric, instability, negative bias temperature instability (NBTI), positive charges, reliability, spatial distribution.

I. INTRODUCTION

TO CONTROL gate leakage, Hf-based dielectric stack has been selected to replace SiON as a gate insulator. In comparison with SiON, Hf-based stacks generally suffer from higher instabilities [1]–[8]. Positive charging causes negative bias temperature instability (NBTI) and limits the lifetime of pMOSFETs, and there is a pressing need for suppressing it. At present, there is little information available on which layer of the stack dominates positive charging, and finding it is the **objective of this letter**. Considering that the quality of Hf oxides and silicates is generally inferior to that of SiON, one may expect that there are more defects in Hf dielectric layers than in interfacial layer (IL) and that the charging can be reduced by using thinner Hf dielectric layers. Early works [5], [6] show that this is indeed the case for as-grown electron traps. However, we will show that positive charges are dominated by the IL and that reducing the HfSiON thickness has little effect on positive charging.

Manuscript received August 21, 2008; revised September 9, 2008. Current version published November 21, 2008. This work was supported by the Engineering and Physical Science Research Council of U.K. under Grant EP/C003071/1. The review of this letter was arranged by Editor C.-P. Chang.

J. F. Zhang, M. H. Chang, Z. Ji, and L. Lin are with the School of Engineering, Liverpool John Moores University, L3 3AF Liverpool, U.K. (e-mail: J.F.Zhang@ljmu.ac.uk; m.h.chang@ljmu.ac.uk; z.ji@2006.ljmu.ac.uk; l.lin@2005.ljmu.ac.uk).

I. Ferain and L. Pantisano are with the IMEC, 3001 Leuven, Belgium (e-mail: Ferain@imec.be; Luigi.Pantisano@imec.be).

G. Groeseneken, S. De Gendt, and M. M. Heyns are with the IMEC, 3001 Leuven, Belgium, and also with the Katholieke Universiteit Leuven, 3001 Leuven, Belgium (e-mail: guido.groeseneken@imec.be; stefan.degentd@imec.be; heyns@imec.be).

Digital Object Identifier 10.1109/LED.2008.2006288

II. DEVICES AND EXPERIMENTS

Hf silicates (80% Hf) were prepared by atomic layer deposition to a thickness of 1, 2, and 3 nm on three IMEC-cleaned wafers. The IL is 1 nm, and the gate is TiN. Both the channel length and width are 1 μm . A slant-etched wafer is also used, with HfSiON fixed at 2 nm and the IL thickness varying between 1.7 and 3.6 nm across the wafer.

The threshold voltage shift ΔV_{th} , was measured by extrapolation with a drain bias of -0.1 V [9]. Both quasi-dc [10] and pulse $I_d \sim V_g$ [11], [12] were used with a measurement time of 6 s and 5 μs , respectively. The ΔV_{th} has two components, namely, a contribution from generated interface states $\Delta V_{\text{th}}(\Delta D_{\text{it}})$, and a contribution from positive charges in dielectric $\Delta V_{\text{th}}(\Delta N_{\text{ot}})$ so that

$$\Delta V_{\text{th}} = \Delta V_{\text{th}}(\Delta D_{\text{it}}) + \Delta V_{\text{th}}(\Delta N_{\text{ot}}).$$

Early works [13], [14] reported that the generated interface states are acceptor-type above the midgap of Si and donor-type below the midgap. As a result, $\Delta V_{\text{th}}(\Delta N_{\text{ot}})$ can be determined from the shift of the gate voltage at the midgap of Si, where the net charge of interface states is negligible. The density of generated interface states was measured from the change in the subthreshold swing [15] and charge pumping (CP).

III. RESULTS AND DISCUSSIONS

To determine the dominant layer for positive charges, three samples with different thicknesses of HfSiON layers were used. The problem is that positive charges increase with the stress level and that a comparison of different samples is meaningful only if they were subjected to the same stress. Under the same effective oxide field, Fig. 1(a) shows that the difference in their density of generated interface states ΔD_{it} is negligible, confirming that they were subjected to the same stress level.

Before assessing the spatial location of ΔN_{ot} in Hf-based stacks, we examine its relative importance to the NBTI-induced ΔV_{th} . Fig. 1(b) shows a comparison of the contributions of ΔN_{ot} and ΔD_{it} to ΔV_{th} . Initially, ΔD_{it} is negligible, and ΔV_{th} is dominated by ΔN_{ot} , considering that there are preexisting defects in the stack [7], [8]. As the stress time increases, the contribution of ΔD_{it} rises and reaches about one third of ΔV_{th} for the last point in Fig. 1(b).

As a first attempt for assessing the spatial distribution of positive charges, we study the case where they are distributed throughout the stack. To simplify the analysis, we assume that

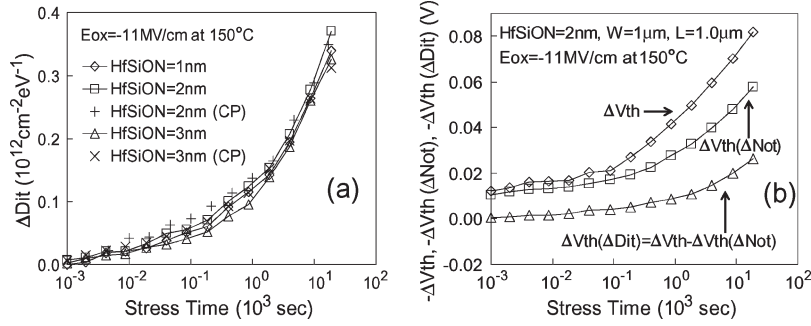


Fig. 1. (a) Density of created interface states ΔD_{it} under $E_{ox} = -11$ MV/cm. $E_{ox} = (V_g - V_{fb} - \Phi_s)/EOT$, where EOT was extracted from the inversion capacitance and where the surface quantization effect has been taken into account. ΔD_{it} measured by CP agrees well with that by the subthreshold swing. (b) Threshold voltage shift ΔV_{th} and its two components, namely, $\Delta V_{th}(\Delta N_{ot})$ and $\Delta V_{th}(\Delta D_{it})$.

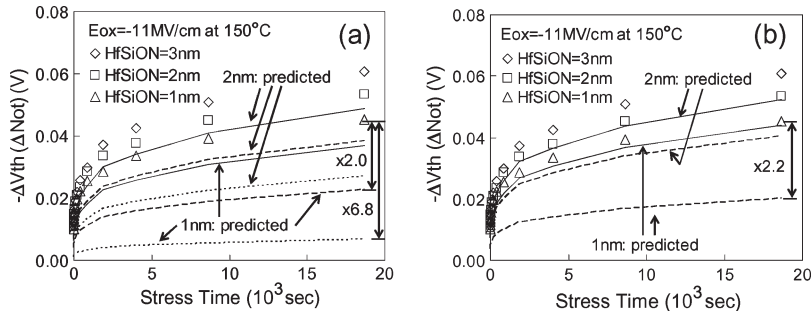


Fig. 2. Comparison of (symbols) test data with the (lines) prediction based on (a) volume and (b) sheet distributions. (a) Prediction is under the following three assumptions: 1) $\rho_{HF} = \rho_{IL}$ (indicated by dashed lines); 2) $\rho_{IF} = 0$ (indicated by dotted lines); and 3) $\rho_{HF} = 0$ (indicated by solid lines). (b) Prediction is under the following two assumptions for positive charges: 1) at the HfSiON/IL interface (indicated by dashed lines); and 2) at the IL/substrate interface (indicated by solid lines). Quasi-dc measurement time is 6 s.

the volume density ρ in both HfSiON and the IL is constant. Although this will not give a detailed spatial distribution, it will allow for the assessment of which layer dominates the positive charges. $\Delta V_{th}(\Delta N_{ot})$ is related to ρ by

$$\Delta V_{th}(\Delta N_{ot}) = -\frac{q \cdot \rho_{HF} \cdot X_{HF}^2}{2 \cdot \epsilon_0 \cdot k_{HF}} - \frac{q \cdot \rho_{IL}}{2 \cdot \epsilon_0 \cdot k_{IL}} \cdot \left[X_{IL}^2 + 2 \cdot \frac{k_{IL}}{k_{HF}} \cdot X_{IL} \cdot X_{HF} \right] \quad (1)$$

where X is the dielectric layer thickness and k is the dielectric constant ($k_{HF} = 16.3$). The subscripts ‘‘HF’’ and ‘‘IL’’ represent HfSiON and IL, respectively. Fig. 2(a) shows a plot the $\Delta V_{th}(\Delta N_{ot})$ measured at different stress times for $X_{HF} = 1, 2,$ and 3 nm. At a given time point, we use $\Delta V_{th}(\Delta N_{ot})$ at $X_{HF} = 3$ nm as the base to predict the $\Delta V_{th}(\Delta N_{ot})$ at $X_{HF} = 1$ and 2 nm under three different assumptions.

A. Uniform Distribution With $\rho_{HF} = \rho_{IL}$

For each $\Delta V_{th}(\Delta N_{ot})$ of $X_{HF} = 3$ nm measured at a given time, $\rho_{HF} = \rho_{IL}$ can be calculated from (1). Once $\rho_{HF} = \rho_{IL}$ is known, $\Delta V_{th}(\Delta N_{ot})$ of $X_{HF} = 1$ and 2 nm at the same time can be predicted by (1). The results are shown as the two dashed lines in Fig. 2(a), and the agreement with the test data is poor. The predicted $\Delta V_{th}(\Delta N_{ot})$ at $X_{HF} = 1$ nm is only half of the measured value.

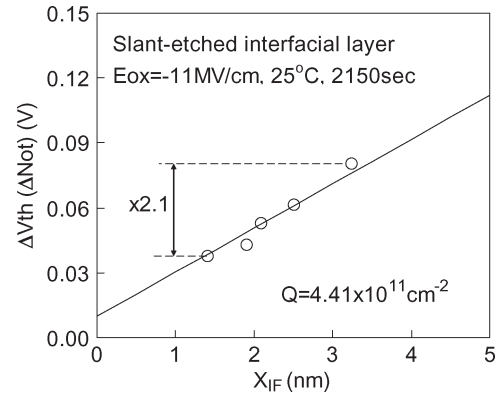


Fig. 3. Effects of IL thickness X_{IF} on $\Delta V_{th}(\Delta N_{ot})$. The HfSiON layer is fixed at 2 nm. The solid line is fitted with (3) by assuming that charges pile up at the substrate interface.

B. All Charges in HfSiON and $\rho_{IL} = 0$

The predicted $\Delta V_{th}(\Delta N_{ot})$ is represented by the two dotted lines, and they depart further from the test data. The predicted $\Delta V_{th}(\Delta N_{ot})$ at $X_{HF} = 1$ nm is only 15% of the test data so that we can rule out that positive charges are dominated by the bulk of HfSiON.

C. All Charges in the IL and $\rho_{HF} = 0$

The predicted $\Delta V_{th}(\Delta N_{ot})$ is represented by the two solid lines, and they are closest to the test data among the three

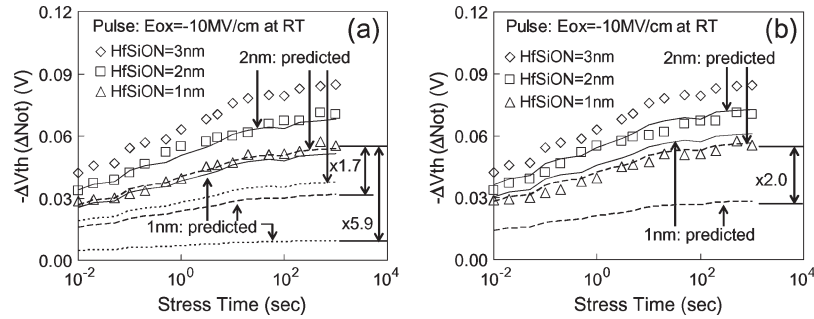


Fig. 4. Comparison of the prediction with the test data based on (a) volume and (b) sheet distributions. The symbols and lines have the same meaning as those in Fig. 2; here, however, the pulsed measurement was used with a measurement time of $5 \mu\text{s}$.

assumptions. This supports that the IL dominates the positive charges. To further improve the agreement between the prediction and test data, we explore the sheet distribution next.

In comparison with conventional MOSFETs with SiON as the gate dielectric, one new feature for a Hf-based stack is the presence of a HfSiON/IL interface, and we examine whether positive charges pile up at this interface. If we assume that all charges are at the HfSiON/IL interface with an area density of Q , we have

$$\Delta V_{\text{th}}(\Delta N_{\text{ot}}) = -\frac{q \cdot X_{\text{HF}} \cdot Q}{\epsilon_0 \cdot k_{\text{HF}}}. \quad (2)$$

The predicted value is shown as the two dashed lines in Fig. 2(b), and it is less than half of the test data for $X_{\text{HF}} = 1 \text{ nm}$. Equation (2) also requires $\Delta V_{\text{th}}(\Delta N_{\text{ot}})$ to be independent of the IL thickness. This is against our test results in Fig. 3 that shows $\Delta V_{\text{th}}(\Delta N_{\text{ot}})$ increasing for thicker IL. We conclude that positive charges are not concentrated at the HfSiON/IL interface.

After ruling out the HfSiON/IL interface, it is natural to study if positive charges pile up at the IL/Si interface. By assuming all charges at the substrate interface, we have

$$\Delta V_{\text{th}}(\Delta N_{\text{ot}}) = -qQ \left(\frac{X_{\text{IL}}}{\epsilon_0 k_{\text{IL}}} + \frac{X_{\text{HF}}}{\epsilon_0 k_{\text{HF}}} \right). \quad (3)$$

The predicted value is shown as the two solid lines in Fig. 2(b), and a good agreement with the test data is achieved. This supports that positive charges pile up at the IL/substrate interface and that, consequently, reducing the HfSiON thickness has little effect on positive charging. The smaller measured $\Delta V_{\text{th}}(\Delta N_{\text{ot}})$ at $X_{\text{HF}} = 1 \text{ nm}$ in Fig. 2(b) results from a larger gate capacitance when compared with that at $X_{\text{HF}} = 3 \text{ nm}$. To explain this pileup, it should be noted that the oxygen vacancy $\equiv \text{Si}-\text{Si} \equiv$ has been proposed as the main source for positive charges [16]. It is reasonable to assume that there are more $\equiv \text{Si}-\text{Si} \equiv$ when moving from a dielectric toward a silicon substrate. Our data, however, do not give direct information on the origin or microscopic structure of positive charges.

The results in Fig. 2 were obtained under an electrical field over the equivalent oxide thickness of $E_{\text{ox}} = -11 \text{ MV/cm}$ and at $150 \text{ }^\circ\text{C}$. The question is whether the dominant layer is sensitive to the stress conditions. We have checked it with

E_{ox} in the range between -11 and -18 MV/cm and a temperature between room temperature and $150 \text{ }^\circ\text{C}$. Our results (not shown) confirm that in all stress conditions, the result is similar to that shown in Fig. 2. To test the impact of the measurement time, it is reduced from 6 s , in Fig. 2, to $5 \mu\text{s}$, in Fig. 4, by using the pulse $I_d \sim V_g$ [11], [12]. Fig. 4 shows that IL still dominates the positive charges, when the recovery is suppressed.

IV. CONCLUSION

In this letter, the dominant layer for the stress-induced positive charge in Hf-based stacks is assessed by varying the thicknesses of HfSiON and ILs. We conclude that positive charges in the stack are dominated by the IL. It is ruled out that positive charges pile up at the HfSiON/IL interface. The results support that positive charges are located close to the IL/substrate interface. Consequently, unlike electron trapping, a reduction of the HfSiON thickness will not reduce the positive charges.

REFERENCES

- [1] T. P. Ma, H. M. Bu, X. W. Wang, L. Y. Song, W. He, M. Wang, H.-H. Tseng, and P. J. Tobin, "Special reliability features for Hf-based high- κ gate dielectrics," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 1, pp. 36–44, Mar. 2005.
- [2] M. Houssa, S. De Gendt, J. L. Autran, G. Groeseneken, and M. M. Heyns, "Role of hydrogen on negative bias temperature instability in HfO₂-based hole channel field-effect transistors," *Appl. Phys. Lett.*, vol. 85, no. 11, pp. 2101–2103, Sep. 2004.
- [3] H. R. Harris, R. Choi, B. H. Lee, C. D. Young, J. H. Sim, K. Mathews, P. Zeitzoff, P. Majhi, and G. Bersuker, "Comparison of NMOS and PMOS stress for determining the source of NBTI in TiN/HfSiON devices," in *Proc. 43rd Int. Rel. Phys. Symp.*, 2005, pp. 80–83.
- [4] C. Z. Zhao, J. F. Zhang, M. B. Zahid, B. Govoreanu, G. Groeseneken, and S. De Gendt, "Determination of capture cross sections for as-grown electron traps in HfO₂/HfSiO stacks," *J. Appl. Phys.*, vol. 100, no. 9, p. 093 716, Nov. 2006.
- [5] J. F. Zhang, C. Z. Zhao, M. B. Zahid, G. Groeseneken, R. Degraeve, and S. De Gendt, "An assessment of the location of as-grown electron traps in HfO₂/HiSiO stacks," *IEEE Electron Device Lett.*, vol. 27, no. 10, pp. 817–820, Oct. 2006.
- [6] J. H. Sim, S. C. Song, P. D. Kirsch, C. D. Young, R. Choi, D. L. Kwong, B. H. Lee, and G. Bersuker, "Effects of ALD HfO₂ thickness on charge trapping and mobility," *Microelectron. Eng.*, vol. 80, pp. 218–221, Jun. 2005.
- [7] C. Z. Zhao, M. B. Zahid, J. F. Zhang, G. Groeseneken, R. Degraeve, and S. De Gendt, "Threshold voltage instability of p-channel metal-oxide-semiconductor field effect transistors with hafnium based dielectrics," *Appl. Phys. Lett.*, vol. 90, no. 14, p. 143 502, Apr. 2007.

- [8] C. Z. Zhao, J. F. Zhang, M. H. Chang, A. R. Peaker, S. Hall, G. Groeseneken, L. Pantisano, S. De Gendt, and M. Heyns, "Stress-induced positive charge in Hf-based gate dielectrics: Impact on device performance and a framework for the defect," *IEEE Trans. Electron Devices*, vol. 55, no. 7, pp. 1647–1656, Jul. 2008.
- [9] J. F. Zhang, M. H. Chang, and G. Groeseneken, "Effects of measurement temperature on NBTI," *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 298–300, Apr. 2007.
- [10] J. F. Zhang, H. K. Sii, G. Groeseneken, and R. Degraeve, "Hole trapping and trap generation in the gate silicon dioxide," *IEEE Trans. Electron Devices*, vol. 48, no. 6, pp. 1127–1135, Jun. 2001.
- [11] T. Yang, M. F. Li, C. Shen, C. H. Ang, C. Zhu, Y.-C. Yeo, G. Samudra, S. C. Rustagi, M. B. Yu, and D. L. Kwong, "Fast and slow dynamic NBTI components in p-MOSFET with SiON dielectric and their impact on device life-time and circuit application," in *VLSI Symp. Tech. Dig.*, 2005, pp. 92–93.
- [12] J. F. Zhang, J. F. Zhang, Z. Ji, M. H. Chang, B. Kaczer, and G. Groeseneken, "Real V_{th} instability of pMOSFETs under practical operation conditions," in *IEDM Tech. Dig.*, Dec. 2007, pp. 817–820.
- [13] G. A. Scoggan and T. P. Ma, "Effects of electron-beam radiation on MOS structures as influenced by the silicon dopant," *J. Appl. Phys.*, vol. 48, no. 1, pp. 294–300, Jan. 1977.
- [14] J. F. Zhang, S. Taylor, and W. Eccleston, "Electron trap generation in thermally grown SiO₂ under Fowler–Nordheim stress," *J. Appl. Phys.*, vol. 71, no. 2, pp. 725–734, Jan. 1992.
- [15] C. Tan, M. Xu, and Y. Wang, "Application of the difference subthreshold swing analysis to study generation of interface traps in MOS structures due to Fowler–Nordheim aging," *IEEE Electron Device Lett.*, vol. 15, no. 7, pp. 257–259, Jul. 1994.
- [16] H. S. Witham and P. M. Lenahan, "Nature of the E deep hole trap in metal–oxide–semiconductor oxides," *Appl. Phys. Lett.*, vol. 51, no. 13, pp. 1007–1009, Sep. 1987.