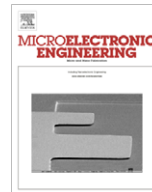




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Defects and instabilities in Hf-dielectric/SiON stacks

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ABSTRACT

In this work, a review on the recent progress in understanding defects and instabilities in Hf-dielectric/SiON stacks will be given for both nMOSFETs and pMOSFETs. The key issues addressed for nMOSFETs include the capture cross section of electron traps, their location and justification of the model used. For pMOSFETs, a framework will be proposed for the defects and then used to interpret the anomalous NBTI kinetics. The dominant dielectric layer for positive charging will be identified. Wherever possible, the classical SiO_2 will be used as a benchmark and the similarity and difference between the stack and SiO_2 will be highlighted. It will be shown that the stack behaves like a degraded SiO_2 .

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1. Introduction

To control gate leakage current, the Hf-dielectric/SiON stack has been selected to replace SiON. When compared with SiON, the stack generally has more defects and is more vulnerable to stress, leading to higher threshold voltage instability, ΔV_{th} [1–4]. The understanding of the defects and instability is incomplete and a review on the recent progress is given here.

For nMOSFETs, ΔV_{th} is dominated by electron trapping [2–4]. Some key properties of the electron traps will be determined, including capture cross sections, density and spatial locations. There have been doubts and confusions [5] on the validity of the first order model used to extract these parameters and its justification will be given. It will be shown that electron traps are preexisting and dominated by the Hf-dielectric layer [4].

For pMOSFETs, the negative bias temperature instability (NBTI) is the main concern [6–9] and a framework will be proposed for the defect [7]. Apart from the generated interface states, there are three types of positive charges in the dielectric: as-grown hole trapping (AHT), cyclic positive charges (CPC) and anti-neutralization positive charges (ANPC) [7]. This framework is then used to interpret the anomalous behavior of NBTI and its kinetics [7,8] and the role of hydrogen will be highlighted. Unlike electron trapping, positive charging is dominated by the interfacial layer (IL) [9].

2. Devices

Both HfO_2 and Hf-silicates were prepared by atomic layer deposition with an EOT from 1.13 to 1.8 nm. The HfO_2 has a physical thickness between 1.8 and 4.0 nm and the physical thickness of silicates is between 1 and 3 nm with 70–80% Hf. The samples were annealed in forming gas at 520 °C for 20 min and have a TaN/TiN gate. The channel length and width is 0.25–1 μm and 10 μm , respectively. The device used for each test is specified in the figure caption or legends.

3. Instability of nMOSFETs

3.1. Domination of pre-existing electron traps

Although there are little pre-existing electron traps in SiO_2 [10,11], they dominate the ΔV_{th} of nMOSFETs with the stack [2–4]. Fig. 1 shows that electron trapping is sensitive to measurement delay and it has to be reduced to tens of microseconds to suppress the loss [2–4]. Electron trapping is insensitive to temperature [2], although it is sometimes referred to as positive bias temperature instability (PBTI).

3.2. Electron fluency, N_{inj}

Before one can determine the effective physical size of electron traps, namely the capture cross section, one must know the

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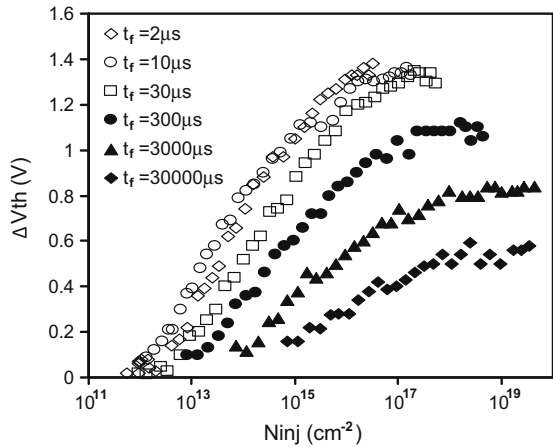


Fig. 1. Effects of measurement time, t_f , on electron trapping. N_{inj} is electron fluency. The stack has a 4 nm HfO₂ [4].

number of electrons available for trapping in the dielectric. Two issues should be addressed here: One is that not every electron passing through the stack can fill traps and it has been reported that trap-assisted tunneling current does not contribute to trapping [2].

The other is that the negative space charge from trapping reduces the field near cathode and in turn the gate current I_g . Fig. 2 shows that I_g can reduce by two orders of magnitude in tens of microseconds [3]. For a quasi-DC parameter analyzer, it takes 10–150 ms for measuring one point, so that it underestimates I_g during the trapping period. If this quasi-DC I_g is used to calculate N_{inj} , N_{inj} will be underestimated by one order of magnitude approximately. This will lead to an overestimation of capture cross section by a factor of 10 and a correction must be made [3].

3.3. Capture cross sections

After determining N_{inj} , a trapping model is needed for extracting the capture cross section, σ . The first order trapping model is well known [3,10]:

$$\Delta N_{eff} = N_{s1} [1 - \exp(-\sigma_1 N_{inj})] + N_{s2} [1 - \exp(-\sigma_2 N_{inj})]. \quad (1)$$

Fig. 3 shows that the two extracted capture cross sections are well separated in the order of $\sigma_1 \sim 10^{-14} \text{ cm}^2$ and $\sigma_2 \sim 10^{-16} \text{ cm}^2$, respectively. The σ is not sensitive to the stress and fabrication

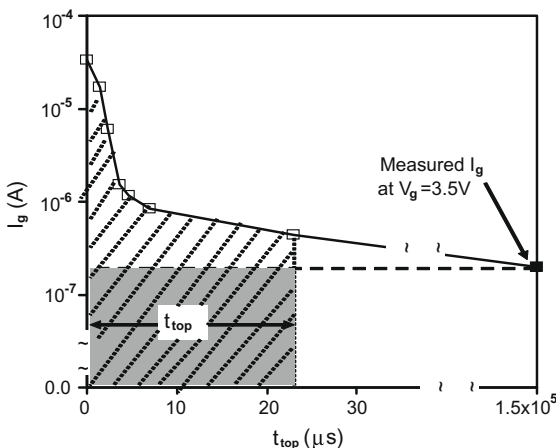


Fig. 2. The calculated transient gate current for $V_g = 3.5 \text{ V}$. Trapping reduces I_g by two orders of magnitude [3]. The stack has a 4 nm HfO₂. The t_{top} is the trapping time.

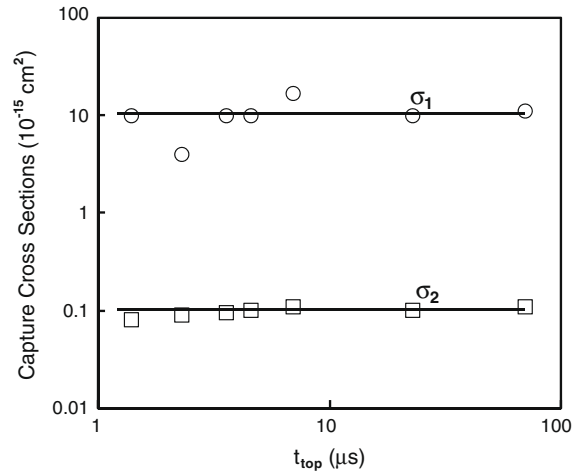


Fig. 3. Capture cross sections for pre-existing electron traps in a 4 nm HfO₂ [3].

conditions, although the trap density is [3]. The two capture cross sections for the pre-existing traps in the stack are similar to those for the electron traps generated in SiO₂ by electrical stress [10,11].

3.4. Justification of the first order trapping model

The first order model of Eq. (1) is in dispute [5] and one may say that the extraction of capture cross sections is a curve-fitting exercise. Supporting evidence is needed to justify it. Fig. 4 shows that the effective density, N_{s1} , for σ_1 can vary independently from the N_{s2} for σ_2 [10]. The N_{s1} increases continuously with stress, whilst N_{s2} saturates. This suggests that electron traps with σ_1 eventually trigger the oxide breakdown [12,13]. The effective size of the defect independently obtained from breakdown tests is indeed in the order of 10^{-14} cm^2 [12,13], agreeing well with σ_1 . Moreover, some processes suppress traps with one capture cross section without affecting the other [14]. These strongly support the first order trapping model.

3.5. Location of pre-existing electron traps

Since there are no pre-existing electron traps in SiON [10,11], two assumptions for their locations in the stack are in the bulk of Hf-dielectric layer or at the Hf-dielectric/SiON interface. To test them, the thickness of Hf-dielectric is varied without changing the

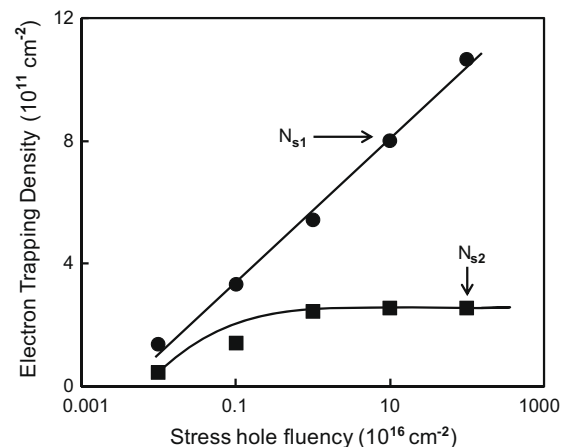


Fig. 4. The effective density of electron traps for σ_1 varies independently from that for σ_2 [10]. The traps were generated in a 7.1 nm SiO₂.

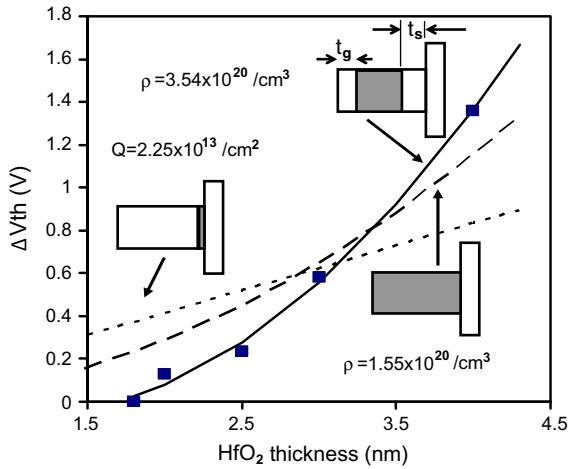


Fig. 5. Location of electron traps in the stack. Grey areas of the energy band diagrams represent the assumed trapping region and lines are fitted according to the assumption. Symbols are test data [4].

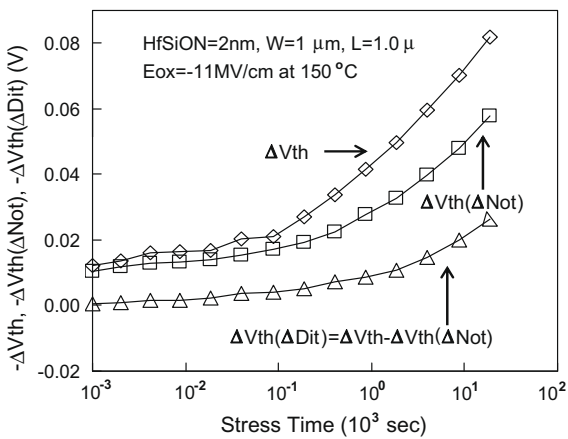


Fig. 6. Contribution of generated interface states, ΔD_{it} , and PC in dielectric, ΔN_{ot} , to NBTI-induced ΔV_{th} [9].

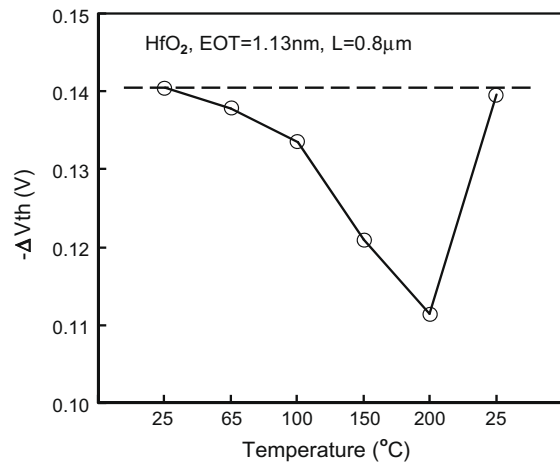
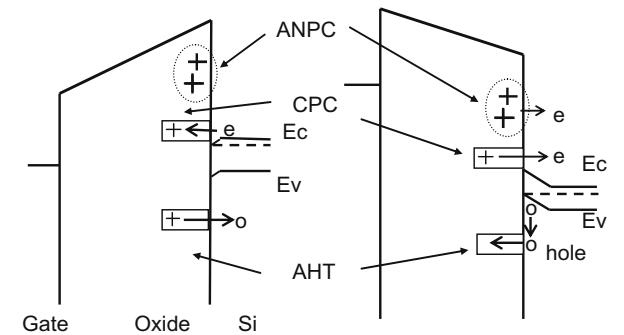
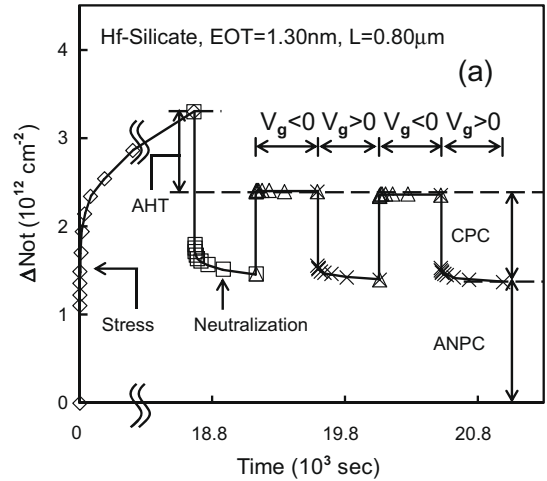


Fig. 7. For a given number of defects, ΔV_{th} reduces for higher measurement temperature that was varied in the order of 25, 65, 100, 150, 200, and then back to 25 °C [7].

interfacial layer (IL). Fig. 5 shows that both assumptions do not agree with the test data. Good agreement is obtained by assuming traps being in the central region of Hf-dielectric layer. As the thick-



(b) $V_g > 0$: Neutralization (c) $V_g < 0$: Charging

Fig. 8. Three types of positive charges. (a) Shows the test sequence. (b) and (c) show their neutralization under $V_g > 0$ and charging under $V_g < 0$. The cyclic positive charge (CPC) has the same charging and discharging rate. The anti-neutralization positive charge (ANPC) is more difficult to neutralize than charging, whilst the opposite applies to the as-grown hole traps (AHT) [7].

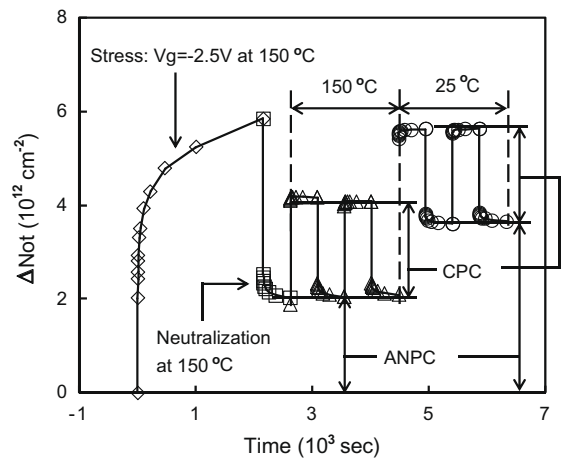


Fig. 9. After stress and measurement at 150 °C, the device was cooled down to 25 °C and measured again. ANPC increases for lower measurement temperature, but CPC does not [7]. The sample is a HfO_2 with EOT = 1.13 nm.

ness of Hf-dielectric reduces to below 2 nm, electron trapping becomes insignificant for a properly processed stack [4,15]. As a result, ΔV_{th} of nMOSFETs can be suppressed and the attention is turned to the instability of pMOSFETs next.

4. Instability of pMOSFETs

4.1. Interface states versus charges in dielectric

Traditionally, it is well known that the generated interface states, ΔD_{it} , and positive charging in gate dielectric, ΔN_{ot} , are equally important for NBTI of SiO_2 [16,17]. The importance of ΔN_{ot} is in dispute for thin SiON [17,18]. For the stack, Fig. 6 shows that ΔN_{ot} is important. To further illustrate its importance, Fig. 7 shows that for a fixed number of defects, ΔV_{th} reduced for higher measurement temperature. Since ΔD_{it} is insensitive to measurement temperature [7], this reduction can only be explained by ΔN_{ot} .

4.2. A framework for defects

It will be shown that ΔN_{ot} has three components and the temperature dependence in Fig. 7 originates from only one of them. In Fig. 8a, NBTI stress was performed first and ΔN_{ot} built up. This was followed by applying $V_g > 0$ and $V_g < 0$ alternatively with $E_{ox} = \pm 5 \text{ MV/cm}$ over EOT. Some positive charges (PC) can be repeatedly neutralized under $V_g > 0$ and recharged under $V_g < 0$, so that they are called as cyclic positive charge (CPC). CPC has an energy level close to E_c (Figs. 8b and c). Part of PC has energy level above E_c , so that their neutralization is more difficult than charging and they are referred to as anti-neutralization positive charge (ANPC). Moreover, the as-grown hole trap (AHT) has energy level below E_v [19], making its neutralization easier than charging, so that the recharging under $V_g < 0$ could not reach the level of NBTI stress [7,20,21].

The neutralization of CPC only involves carrier tunneling at the same energy level, which is insensitive to temperature. However, free electrons must be excited to reach ANPC. The framework predicts less ANPC and the same CPC at higher measurement temperature and this is confirmed by Fig. 9. ANPC must be responsible for the reduction of ΔV_{th} in Fig. 7.

4.3. NBTI kinetics

For SiO_2 , it is well known that NBTI follows a power law [16,17]. Fig. 10a, however, shows a flat region at short time for the stack [8].

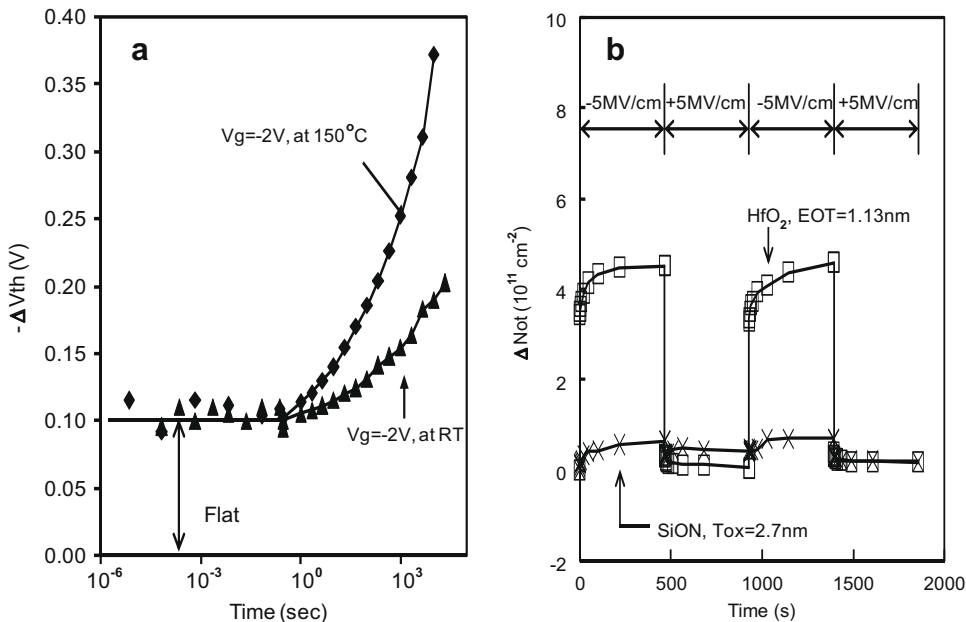


Fig. 10. (a) Anomalous NBTI kinetics of the stack: flat-then-rise. (b) CPC is negligible for a fresh SiON, but can be considerable in a fresh stack [8].

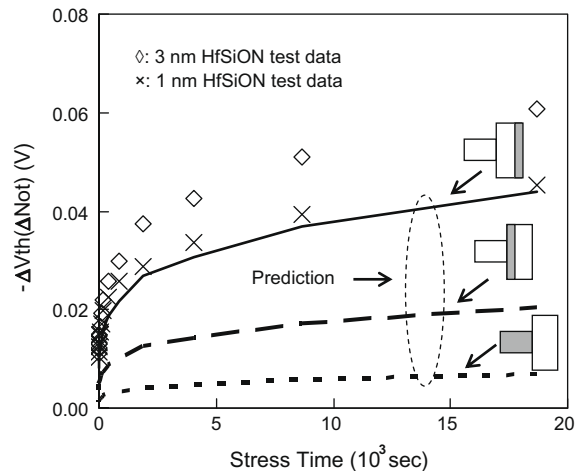


Fig. 11. Location of positive charges in the stack. The lines are the predicted ΔV_{th} for a 1 nm HfSiON stack from the ΔV_{th} of 3 nm HfSiON stack, according to the assumed location (grey regions). Symbols are test data [9].

The proposed framework will be used to identify the defect responsible for this anomalous behavior. Since the flat region is clearly insensitive to temperature, it can originate from either AHT or CPC. For thin layers ($< 3 \text{ nm}$), the deep energy level of AHT leads to a loss of majority of its charges when measurement time increases from microseconds to seconds [17,22]. Since the charging in Fig. 10a remains the same between microseconds and seconds, AHT cannot be responsible for the flat region. It can only originate from CPC and these CPCs are preexisting in the stack, as confirmed by Fig. 10b.

4.4. Dominant layer for positive charging (PC)

Fig. 5 shows that electron trapping is dominated by the central region of Hf-dielectric and ΔV_{th} of nMOSFETs is suppressed by using a sub-2 nm Hf-dielectric layer. To find whether this also applies to NBTI of pMOSFETs, Fig. 11 shows that test data does not agree with the assumptions that PC is dominated by Hf-dielectric

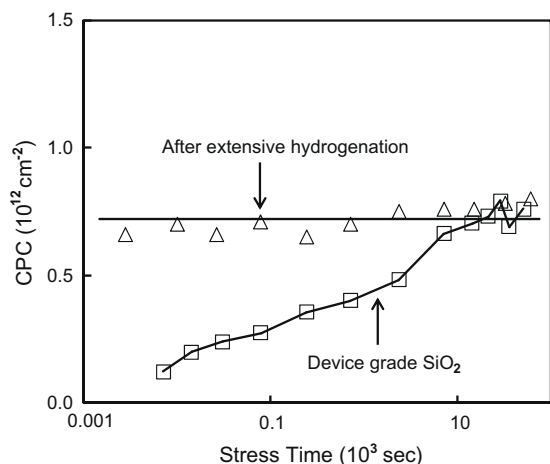


Fig. 12. Dependence of CPC in SiO₂ on stress level. For a device-grade SiO₂, CPC built up gradually with stress. After an extensive hydrogenation, CPC in SiO₂ becomes insensitive to stress and behaves like the stack [24].

or piles up at the Hf-dielectric/IL interface. Good agreement is achieved by assuming that PC is near to the substrate interface [9]. In contrast with electron trapping, a reduction of Hf-dielectric thickness will not reduce PC and NBTI remains a major reliability issue for the stack with sub-2 nm Hf-dielectric layers. The different spatial locations of PC and electron traps also rule out that they originate from the same defect.

4.5. Roles played by hydrogen

Since PC in the stack is dominated by the interfacial SiON layer [9] and it has been suggested that the same mechanism governs the NBTI of the stack and SiO₂ [23], one question is how to explain the large difference in CPC between the stack and the classic SiON shown in Fig. 10b. Hydrogen is widely believed to contribute to PC [24] and one possibility is that the stack suffered from a high level hydrogenation. By increasing the hydrogenation of a SiO₂ layer, one may make it behaving like the stack. Fig. 12 shows that CPC has to be generated by stress in a device-grade SiO₂, leading to a gradual buildup with stress time. After increasing hydrogenation, the CPC in SiO₂ became flat, like the stack behavior.

5. Conclusion

Recent progress in understanding defects and instabilities in Hf-dielectric stacks is reviewed. For nMOSFETs, ΔV_{th} originates mainly from pre-existing electron traps. The trapping follows the first order model and the trapping induced I_g reduction must be corrected in calculating electron fluency. Two well separated capture cross sections are in the order of 10^{-14} cm² and 10^{-16} cm², similar to those for generated electron traps in SiO₂. Trapping is in the central region of Hf-dielectric layer and becomes insignificant for sub-2 nm Hf-dielectric layer.

In contrast, PC is dominated by the IL and NBTI remains important for pMOSFETs. A framework is proposed for PC: cyclic positive charges (CPC), anti-neutralization positive charges (ANPC) and as-grown hole traps. ANPC is the only defect that can explain the increase of $|\Delta V_{th}|$ at lower measurement temperature. Unlike SiO₂, CPC can preexist in the stack, leading to a flat region for NBTI kinetics at short time. This can be caused by a high level hydrogenation of the stack during its fabrication. Overall, the stack behaves like a degraded SiO₂.

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