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Threshold voltage instability of *p*-channel metal-oxide-semiconductor field effect transistors with hafnium based dielectrics

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Threshold voltage V_{th} instability is one major issue for future metal-oxide-semiconductor field effect transistors (MOSFETs) with hafnium (Hf) based gate dielectrics. Previous attention was focused on *n*-channel MOSFETs (nMOSFETs) and the implicit assumption is that it is not important for *p*-channel MOSFETs (pMOSFETs). This work shows that the V_{th} instability of pMOSFETs can be higher than that of nMOSFETs for a sub-2 nm nitrided Hf layer. Unlike nMOSFETs, the V_{th} instability of pMOSFETs is insensitive to measurement time, does not saturate as stress voltage increases, and is not controlled by carrier fluency. Using Hf silicates is less effective in suppressing it. Some speculations are given on the defect and physical processes responsible for the instability. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2719022]

The commercial debut of the hafnium (Hf) based high-*k* layers as gate dielectric has been held back by a number of issues, including low carrier mobility, interaction between gate and high-*k* layer, dielectric breakdown, and threshold voltage V_{th} instability.[1,2] For the V_{th} instability, attention was focused on *n*-channel metal-oxide-semiconductor field effect transistors (nMOSFETs).[1–8] The instability is caused by electron trapping in hafnium oxide[7,8] (HfO_2) and can be suppressed in two ways: using Hf silicates[4] and reducing the thickness of HfO_2 layers.[6,7]

There is little information on the V_{th} instability of *p*-channel MOSFETs (pMOSFETs) and the objective of this work is to fill this knowledge gap. Since the electrons trapped in HfO_2 can be efficiently detrapped under a negative gate bias,[7,8] they are not important for pMOSFETs. This could lead to the expectation that V_{th} instability is always not important for pMOSFETs. We will show that this is not true and positive charge formation can lead to considerable V_{th} instability for pMOSFETs. It is found that the characters of V_{th} instability in pMOSFETs are different from those in nMOSFETs in several aspects. Unlike nMOSFETs, the V_{th} instability of pMOSFETs is insensitive to measurement time, does not saturate as the stress voltage increases, and is not controlled by carrier fluency. The use of Hf silicates is less efficient in suppressing it. Some speculations will be given on the defect and the physical process.

The pMOSFET has a 2 nm HfO_2 layer, prepared by the atomic layer deposition (ALD) with an interfacial layer nitrided in NH_3 at 900 °C for 60 s. The equivalent oxide thickness (EOT) is 1.13 nm and the estimated equivalent interfacial layer thickness (EILT) is 0.73 nm. The gate metal is TaN. A 1 nm Hf silicate (70% Hf) was also prepared and nitrided in NH_3 at 800 °C for 60 s, which gave an EOT of 1.3 nm and an EILT of 0.9 nm. To compare pMOSFETs with nMOSFETs, nMOSFETs were prepared with a 4 nm ALD HfO_2 layer (EOT=1.75 nm and EILT=0.9 nm) or a 1.5 nm Hf silicate (EOT=1.53 nm and EILT=0.9 nm) also nitrided at 800 °C for 60 s in NH_3. The channel length and width for both pMOSFETs and nMOSFETs are 0.25 and 10 μm, respectively.

For nMOSFETs, it is known that the V_{th} instability, ΔV_{th}, is highly dynamic and can be substantially underestimated, if measured from the shift of quasi-dc drain current versus gate bias ($I_d \sim V_g$) characteristics.[3,4,7,8] To suppress the recovery during the measurement, the pulsed $I_d \sim V_g$ technique was developed, which can reduce the delay between stress and measurement to microseconds.[3] We will use the pulsed $I_d \sim V_g$ technique to assess the ΔV_{th} of pMOSFETs. The ΔV_{th} was estimated from the shift of gate bias at a constant drain current of 1.5×10^{-4} A with a drain bias of −0.1 V and a grounded source.

The gate pulse is shown in the inset of Fig. 1, together with the $I_d \sim V_g$ recorded during the two pulse edges. Like nMOSFETs, a "loop" can be seen for the two $I_d \sim V_g$, indicating positive charging during t_{top}. When V_g returns to positive after t_{top}, the positive charge is reneutralized. However, the similarity to nMOSFETs ends here and the important differences are addressed next.

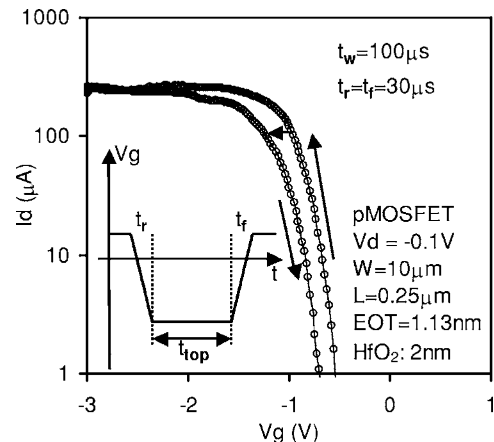

FIG. 1. Instability of pMOSFETs. The inset shows the gate pulse applied and t_w is the pulse width. The transfer characteristics (TCs) during the two edges of the pulse were recorded. The negative shift of the TC results from the positive charge formation in the gate dielectric.

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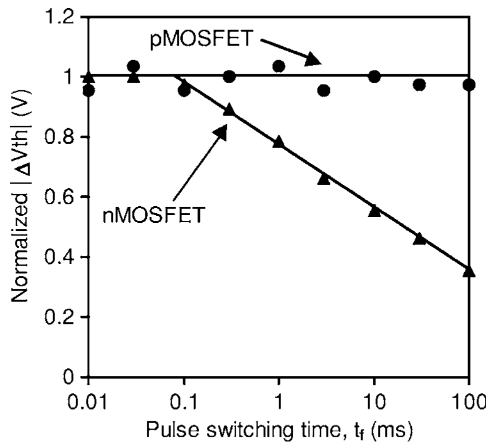

FIG. 2. Dependence of the measured threshold voltage instability, ΔV_{th}, on the measurement time. The measurement time is controlled by the pulse switching time t_f shown in the inset of Fig. 1. Unlike nMOSFETs, the V_{th} instability of pMOSFETs is insensitive to the measurement time. The solid lines are guides for the eyes.

The delay between stress and measurement is controlled by the second edge of the pulse, t_f, in the inset of Fig. 1. As t_f increases, Fig. 2 shows that the ΔV_{th} of nMOSFETs decreases progressively, but the ΔV_{th} of pMOSFETs changes little. This implies that the positive charges in pMOSFETs are more stable than the trapped electrons in nMOSFETs.

The filled symbols in Fig. 3 show that the ΔV_{th} of nMOSFETs can be suppressed by using Hf silicates, agreeing with early work.[4] However, the open diamond symbols show that considerable ΔV_{th} can be present for the pMOSFET with Hf silicate, which is higher than that in the nMOSFET of Hf silicate. For pure SiO_2 or SiON, it is well known that as-grown electron traps are negligible.[9,10] However, a substantial amount of as-grown hole traps exist.[11,12] As a result, it is not surprising that adding Si to high-k layer is less effective for suppressing positive charging.

V_{gs} is the gate voltage during t_{top} in Fig. 1. Figure 3 shows that the ΔV_{th} of nMOSFETs saturates at higher V_{gs}.

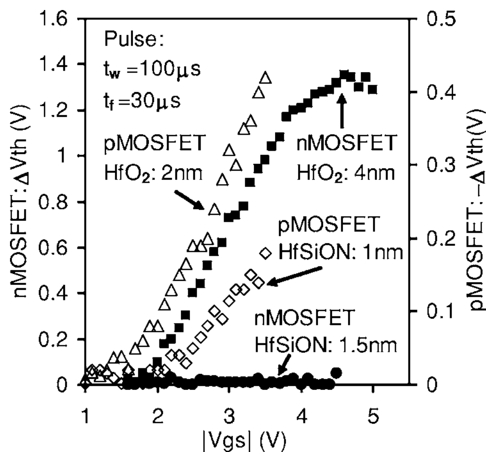

FIG. 3. Dependence of ΔV_{th} on the stress gate voltage and the impact of using Hf silicates. V_{gs} is the bias level during the period of t_{top}, as shown in Fig. 1. The filled symbols represent nMOSFETs and the ΔV_{th} saturates as V_{gs} increases. The instability is negligible in the nMOSFETs with a sub-2-nm Hf silicate. The open symbols represent pMOSFETs and the ΔV_{th} does not saturate with V_{gs} and considerable instability occurs in a sub-2-nm Hf silicate.

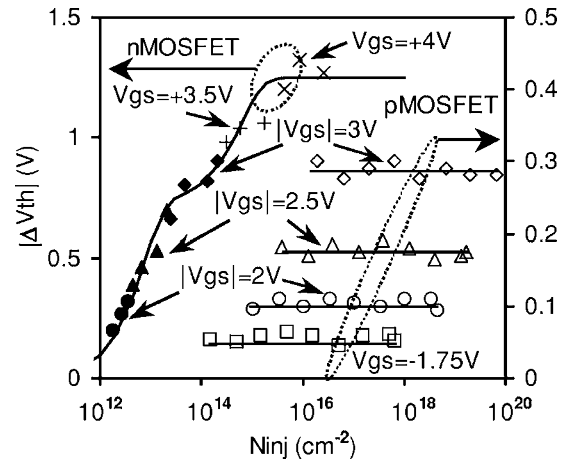

FIG. 4. Dependence of ΔV_{th} on the carrier fluency injected into the gate HfO_2, N_{inj}. Under a constant V_{gs}, the ΔV_{th} of pMOSFETs is insensitive to N_{inj}, but ΔV_{th} of nMOSFETs increases with N_{inj}. Each symbol represents results obtained at a given V_{gs}. The open symbols represent pMOSFETs. The filled symbols and "+" and "×" represent nMOSFETs. V_{gs} and ΔV_{th} are negative for pMOSFETs and positive for nMOSFETs. The different N_{inj} at a given V_{gs} was obtained by varying the time t_{top} shown in Fig. 1. The lines are guides for the eyes.

This is because, once all as-grown electron traps were filled, V_{th} will not shift further. Such a saturation cannot be observed for pMOSFETs.

Since saturation cannot be observed for pMOSFETs, it is possible that a new defect is created. If this is true, ΔV_{th} should increase with the fluency of carriers injected into the dielectric, N_{inj}.[13] Figure 4, however, shows that the ΔV_{th} of pMOSFETs does not increase with N_{inj}. As a result, the instability of pMOSFETs should originate from as-grown defects. Next, we attempt to explain why the instability neither saturates nor increases with N_{inj}.

For nMOSEFTs, electron traps are initially neutral[8,14] and have to capture injected electrons to be charged. Figure 4 shows that N_{inj} controls ΔV_{th}.[7] For pMOSFETs, the insensitivity to N_{inj} suggests that the charging does not involve capturing injected carriers. The charging of two types of defects does not require capturing injected carriers: donorlike defects in the dielectric and the generated interface states. Figure 5 illustrates the charging of donorlike defect. For a fresh device, it is neutral. Under $V_{gs}<0$, its energy level rises above the bottom edge of the silicon conduction band, E_c, and becomes positively charged. The higher $|V_{gs}|$, the more defects

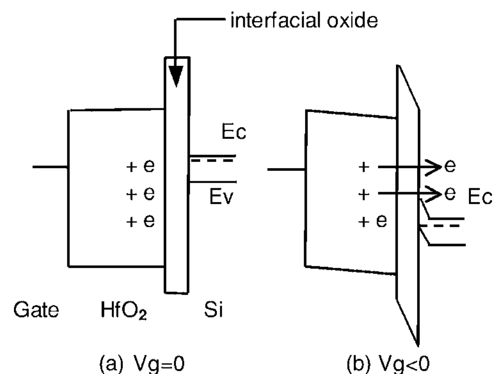

FIG. 5. Schematic illustration of the defect and physical process responsible for the ΔV_{th} of pMOSFETs. Under $V_g=0$, the donorlike defects are neutral (a). Under $V_g<0$, electrons tunnel away, leaving positive charges in the dielectric (b).

move above E_c and, consequently, the more positive charging. This explains the nonsaturation of ΔV_{th} for pMOSFETs.

The creation of interface states by negative bias temperature stress is well known for SiO_2 (Ref. 15) and SiON.[16] The capacitance-voltage measurement (not shown), however, indicates that it is insignificant under the present test condition. This is because the stress time used here is too short (<1 s) to create a considerable amount of interface states but long enough to charge the as-grown defects in the Hf dielectrics investigated here. It is noted that the stress time used for SiO_2 and SiON is typically much longer (e.g., 10^3-10^5 s).[15,16]

In summary, this work shows that the V_{th} instability of pMOSFETs can be higher than that of nMOSFETs for a sub-2-nm nitrided Hf layer. The characters of V_{th} instability of pMOSFETs are different from those of nMOSFETs in several aspects. The measured V_{th} instability reduces significantly as the measurement time increases for nMOSFETs, but not for pMOSFETs. As the magnitude of stress gate voltage increases, the instability saturates for nMOSFETs, but it does not for pMOSFETs. The carrier fluency can control the instability of nMOSFETs, but not that of pMOSFETs. It is speculated that the V_{th} instability of pMOSFETs originates from donorlike defects. Using Hf silicates is less effective in suppressing the instability of pMOSFETs. The V_{th} instability of pMOSFETs reported here is sensitive to nitridation condition, which should be carefully controlled for process optimization.

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