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Process-induced positive charges in Hf-based gate stacks

C. Z. Zhao,[a] J. F. Zhang,[b] and M. H. Chang
School of Engineering, Liverpool John Moores University, Byrom Street, Liverpool L3 3AF, United Kingdom

A. R. Peaker
Centre for Electronic Materials, University of Manchester, Sackville Street, Manchester M60 1QD, United Kingdom

S. Hall
Department of Electrical Engineering and Electronics, University of Liverpool, Brownlow Hill, Liverpool L69 3GJ, United Kingdom

G. Groeseneken,[c] L. Pantisano, S. De Gendt,[c] and M. Heyns[c]
IMEC, Kapeldreef 75, B3001 Leuven, Belgium

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Hf-based gate stacks will replace SiON as a gate dielectric even though our understanding of them is incomplete. For an unoptimized SiO_2 layer, an exposure to H_2 at a temperature over 450 °C can lead to positive charging. In this work, we will show that a thermal exposure of Hf-based gate stacks to H_2 can also induce a large amount of positive charge ($\sim 10^{13}$ cm^{-2}). There is little information available on this process-induced positive charge (PIPC) and the objective of this work is to fill this knowledge gap. The work is divided into two parts: an investigation of the features and properties of PIPC, followed by an exploration of its dependence on process conditions. It will be shown that PIPC does not originate from the generation of interface states, is stable both thermally and electrically, and has a large sample-to-sample variation. It consists of two components: fixed and mobile. Regarding its dependence on process conditions, PIPC occurs in both HfO_2 and Hf-silicate stacks, in devices with either TaN or poly-Si gates, and in both *p* metal-oxide-semiconductor field-effect transistors (*p*MOSFETs) and *n*MOSFETs. PIPC is generally enhanced by nitridation, although it can also be observed in some Hf-based gate stacks without nitridation. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2826937]

I. INTRODUCTION

As the gate SiON approaches 1 nm, it runs out of atoms and the gate leakage current becomes intolerable. The Hf-based dielectric stack has a higher dielectric constant than SiON, allows a thicker layer to be used, and, consequently reduces gate current by orders of magnitude.[1] It has been selected as the gate dielectric for complementary metal-oxide-semiconductor (CMOS) technologies. When compared with devices with a SiON gate dielectric, devices with Hf-based gate stacks suffer from higher instability[1–5] and lower channel carrier mobility.[6,7]

On the instability, an Hf-based gate stack behaves like an inferior or electrically stressed SiO_2 in terms of both electron trapping and positive charging. For electron trapping, it was reported that as-grown trap density reached the order of 10^{13} cm^{-2} for a 4 nm HfO_2 layer,[4] while it is well known that as-grown electron traps are negligible in a modern SiON film.[8,9] The most important signature of the traps is their capture cross sections, and these as-grown electron traps in HfO_2 have similar capture cross sections to those generated by electrical stress in SiO_2.[4,8] For positive charging, it was reported that some defects could be repeatedly neutralized under a positive gate bias and recharged under a negative gate bias.[5,10,11] They are referred to as "cyclic positive charges" (CPCs) and their charging and neutralization only involve carrier tunneling between the defect and substrate at the same energy level. For SiO_2, CPC is absent in a fresh sample and only appears after electrical stress.[10,11] For HfO_2, CPC was observed even in a fresh sample.[5]

Electrical stress is not the only way to charge the gate dielectric. For an inferior SiO_2, it was reported that an exposure to H_2 at a temperature of 450 °C or above could lead to substantial positive charging.[12–16] This process-induced positive charging (PIPC) has been observed for both the buried oxide in a silicon-on-insulator structure[13,14] and some unoptimized gate SiO_2.[16] It is typically absent for a device-grade gate SiO_2. An exposure of SiO_2 to a temperature of 1100 °C or above enhances the positive charging.[12] Although an Hf-based gate stack does not experience such a high temperature in a typical CMOS process, it does not rule out that PIPC can take place, because an Hf-based gate stack often behaves like an inferior SiO_2. PIPC has been observed for Al_2O_3,[17] but there is little information on Hf-based oxide layers.

In this work, we will show that PIPC can occur in a typical Hf-based gate stack. The objective is twofold: to investigate the features and properties of the PIPC and to explore its dependence on process conditions. After a description of devices and experiments in Sec. II, the features and

[a]Present address: University of Liverpool, Liverpool, UK.
[b]Electronic mail: j.f.zhang@ljmu.ac.uk.
[c]Also at KU Leuven, Leuven, Belgium.

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77 properties of PIPC are compared with the stress-induced
78 positive charges (SIPCs) in Sec. III. It is found that PIPC
79 originates from charges in dielectric rather than interface
80 states. Unlike SIPC, PIPC is stable both electrically and ther-
81 mally. It has two components: mobile and fixed. The mobile
82 charge can be shifted within the dielectric stack by the elec-
83 trical field, but its numbers remain constant. In contrast with
84 the uniform SIPC, PIPC has a large sample-to-sample varia-
85 tion. In Sec. IV, the impact of process conditions on PIPC
86 will be studied. This includes hydrogenation, type of gate
87 material, conduction channel polarity, nitridation, source/
88 drain activation, and replacing HfO_2 by Hf-silicates. It is
89 found that hydrogen plays an active role in PIPC and nitri-
90 dation enhances the positive charging.

91 II. DEVICES AND EXPERIMENTS

92 A. Devices

93 *p* metal-oxide-semiconductor field-effect transistors
94 (*p*MOSFETs) and *n*MOSFETs fabricated from eight differ-
95 ent batches were tested in this work. Fabrication typically
AQ: #1 96 starts with an IMEC clean and a 0.4–1 nm chemical SiO_2.[18]
97 For some devices, this interfacial layer was nitrided in NH_3
98 at 900 °C for 60 s before depositing HfO_2. Both HfO_2 and
99 Hf silicates were prepared by atomic layer deposition with an
100 equivalent oxide thickness (EOT) in the range from 0.96 to
101 1.8 nm. The silicates have an Hf concentration between 70%
102 and 80% and were nitrided either in NH_3 at 800 °C for 60 s
103 or in decoupled plasma. A 1000 °C spike was typically used
104 to activate the source and drain, but there are also samples
105 where the activation was by solid phase epitaxial regrowth at
106 650 °C for 1 min. The gate material is either poly-Si or TaN
107 capped by TiN, and the devices received a forming gas an-
108 neal at 520 °C for 20 min. The channel length and width are
109 0.25–1 μm and 10 μm, respectively. Details of the device
110 used for each test are given in the figure legend or caption.

111 B. Experiments

112 The test sequence starts with measuring the transfer
113 characteristic (TC) at a drain bias of 0.1 V. The device was
114 then exposed to a typical temperature of 500 °C for 30 min
115 in either forming gas (FG, 10% H_2) or N_2. After the expo-
116 sure, TC was measured again and the shift in TC was moni-
117 tored from the change of gate bias at a constant drain current
118 of 10^{-6} A. Since the spatial distribution of PIPC is not
119 known, we follow the well accepted practice by assuming
120 the charge centroid is at the dielectric/substrate interface[19,20]
121 and use the "effective charge density," ΔN_{ot}. ΔN_{ot} was evalu-
AQ: #2 122 ated from the shift of gate voltage at the midband of
123 silicon.[4,8] The initial interface state density is in the order of
124 10^{10} cm^{-2} eV^{-1} and the generated interface states were mea-
125 sured from the change in the subthreshold swing.[21,22] To as-
126 sess the mobile positive charge component, the gate bias
127 polarity was alternated with an effective oxide field over the
128 EOT of $E_{ox}(EOT)=\pm 5$ MV/cm.
129 To facilitate the comparison with the SIPCs, the gate
130 bias, V_g, was typically ramped from +1 to −2.5 V and then
131 back. The transfer characteristics of *p*MOSFETs correspond-
132 ing to the two V_g ramps were recorded. The SIPC can typi-

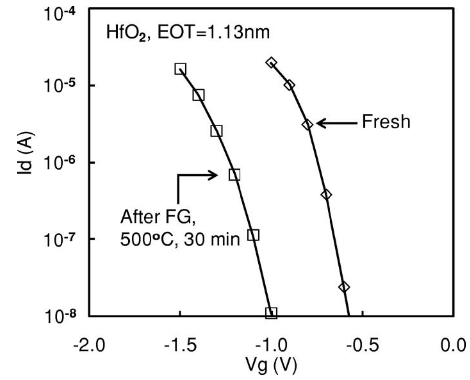

FIG. 1. PIPC formation. The FG (10% H_2) anneal was at 500 °C for 30 min. The sample was nitrided in NH_3 at 900 °C for 60 s before depositing a 2 nm HfO_2 layer. The *p*MOSFET has a TaN gate.

cally be observed from a negative shift of the TC. 133
*n*MOSFETs were not used here since the positive gate bias 134
required for switching them on would neutralize SIPC. All 135
measurements were carried out at room temperature. 136

III. FEATURES AND PROPERTIES 137

A. Charges in Hf-based gate stacks versus interface states 138 139

Figure 1 shows the typical transfer characteristics, I_d 140
$-V_g$, before and after an exposure to the FG at 500 °C for 30 141
min. The negative shift indicates positive charge formation 142
with an effective density, ΔN_{ot}, of 10^{13} cm^{-2}. The thermal 143
exposure also induces an increase of the work function of 144
TaN gate,[23] leading to a positive shift of I_d-V_g. The magni- 145
tude of this shift is only about 10% of that shown in Fig. 1 146
and is in the opposite direction, as will be presented in Sec. 147
IV D. As a result, the work function increase of TaN is not 148
responsible for the shift in Fig. 1. The compensation effect of 149
the work function increase of TaN on positive charging was 150
taken into account when PIPC was evaluated in this work. 151
Figure 2 shows that the PIPC is thermally activated. It 152
also compares the variation of interface states induced by the 153
thermal exposure, ΔD_{it}, with ΔN_{ot}. It is obvious that ΔN_{ot} is 154

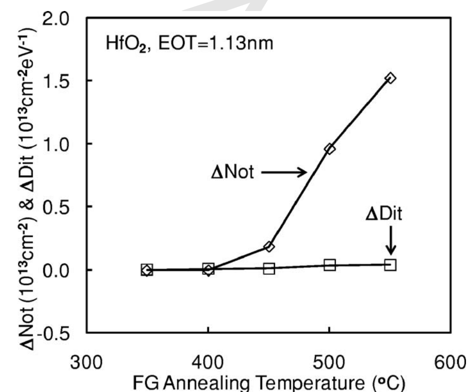

FIG. 2. A comparison of the effective density of positive charge in gate dielectric, ΔN_{ot}, with the generated interface state density, ΔD_{it}. The FG exposure time is 30 min at each temperature. The positive charging is thermally activated and $\Delta N_{ot} \gg \Delta D_{it}$. The sample used is the same as that in Fig. 1.

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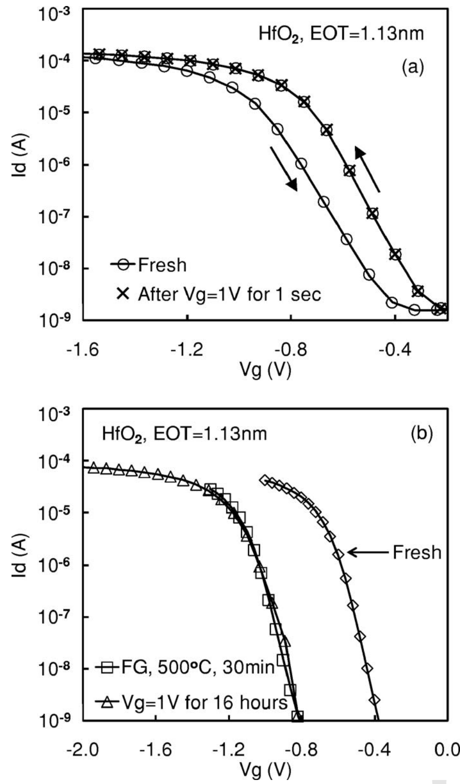

FIG. 3. Electrical stability of (a) SIPC and (b) PIPC. In (a), the gate bias, V_g, was first ramped to −2.5 V and held at −2.5 V for 0.15 s for positive charging and then ramped back to +1 V. The loop in the two drain current, I_d, vs V_g characteristics is caused by the SIPC. After V_g was kept at +1 V for 1 s, it was ramped in the negative direction again and the symbol × shows that the SIPC was neutralized. In (b), $V_g = +1$ V was applied for 16 h after the PIPC formation. When $I_d - V_g$ was measured again, the symbol △ indicates that the PIPC changed little. In contrast with SIPC, PIPC is highly stable under $V_g > 0$. The sample used is the same as that in Fig. 1.

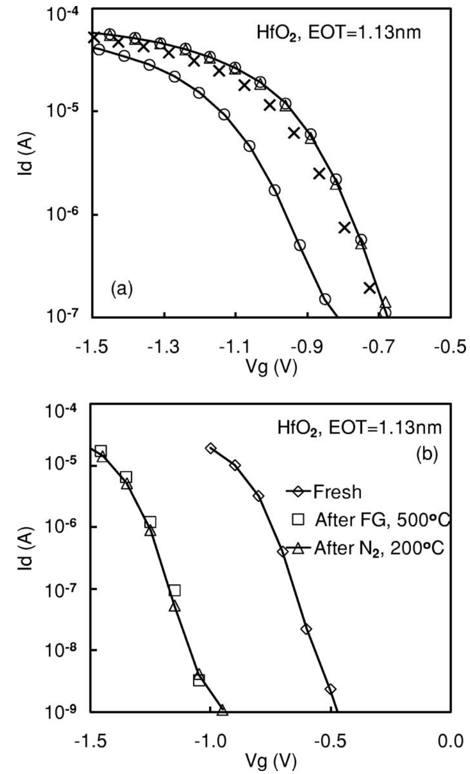

FIG. 4. Thermal stability of (a) SIPC and (b) PIPC. In (a), V_g was ramped from +1 to −2.5 V and then back to form SIPC (○) on one device. For another device, V_g was ramped from +1 to −2.5 V, and then annealed at 200 °C for 5 min in N_2 with all terminals floating, before being ramped back from −2.5 to +1 V (×). The SIPC is thermally unstable. In (b), after forming PIPC, the device was annealed at 200 °C for 16 h in N_2 with all terminals floating. When $I_d - V_g$ was monitored again, the symbol △ indicates that the PIPC changed little. In contrast with SIPC, PIPC is thermally stable. The sample used is the same as that in Fig. 1.

155 much higher than ΔD_{it}. As a result, PIPC is dominated by 156 charge within the gate dielectric. Its spatial location is not 157 known at present.

158 B. Stability

159 It is well known that the SIPCs in a thin gate dielectric 160 can be highly unstable.[22] Figure 3(a) shows that an applica- 161 tion of $V_g = -2.5$ V leads to a loop in the $I_d - V_g$ characteris- 162 tics as a result of positive charge formation. The SIPC is 163 neutralized by applying $V_g = +1$ V for 1 s. To test if the 164 PIPC can also be neutralized under a positive gate bias, V_g 165 $= +1$ V was applied after the thermal exposure in Fig. 3(b). 166 In contrast with the SIPC, PIPC changed little after 16 h. The 167 electron tunneling from the substrate cannot neutralize PIPC, 168 possibly because it has an energy level above that of tunnel- 169 ing electrons.

170 After examining the charging stability against gate bias, 171 we now study its thermal stability. On the one hand, Fig. 4(a) 172 shows that SIPC can be readily removed by a 5 min anneal at 173 200 °C in N_2 with all terminals floating. On the other hand, 174 Fig. 4(b) shows that PIPC cannot be neutralized even after 175 16 h at 200 °C. We conclude that, unlike SIPC, PIPC is 176 highly stable.

C. Fixed and mobile positive charges 177

For SiO_2, PIPC has two components: mobile and fixed 178 positive charges.[12,16] To investigate whether PIPC also has 179 two components for Hf-based gate stacks, the gate bias po- 180 larity was alternated in Fig. 5(a) with an equivalent oxide 181 field, $E_{ox}(\mathrm{EOT}) = \pm 5$ MV/cm. As illustrated in Fig. 5(b), the 182 mobile positive charge (MPC) was pushed toward the sub- 183 strate under $V_g > 0$ and its effect on V_{th} increases, leading to 184 a rise of $|\Delta V_{th}|$. The opposite occurs under $V_g < 0$. It should 185 be pointed out that the amount of MPC remained constant 186 when they were cycled within the stack. Figure 5(a) also 187 shows that part of the PIPC does not change with gate bias 188 polarity and they are fixed positive charges (FPCs). The ratio 189 of MPC against total PIPC is typically around 10%. 190

It is interesting to compare the process-induced MPC 191 with the stress-induced CPC.[5,10,11] Figure 6(a) shows that 192 under $V_g > 0$, the CPC-induced $|\Delta V_{th}|$ was actually reduced, 193 opposite to the MPC-induced increase in Fig. 5(a). This is 194 because electrons can tunnel into the dielectric and neutralize 195 the CPC, as illustrated in Fig. 6(b). The alternation of gate 196 bias polarity changes the density of SIPCs in Hf-based gate 197 stacks. In contrast, it only changes the location of process- 198 induced MPC. 199

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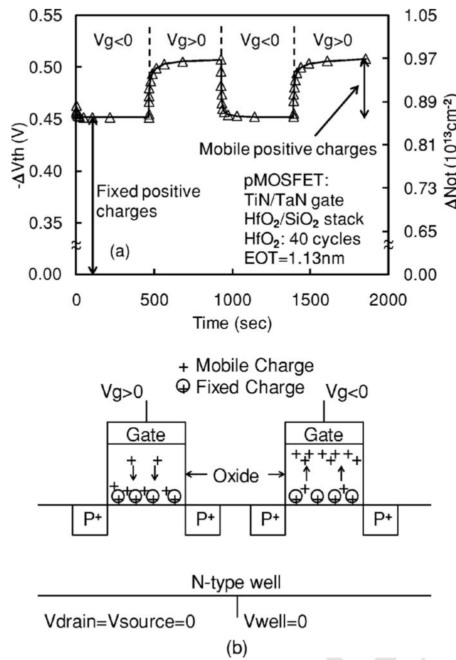

FIG. 5. Two components of PIPC: mobile and fixed positive charges. In (a), the device was exposed to FG at 500 °C for 30 min. (b) illustrates that under $V_g>0$, mobile positive charges were pushed toward the substrate, resulting in a higher $|\Delta V_{th}|$. The V_g polarity changes the location of mobile charges, but their number remains constant. A part of the charges is not affected by the alternation of gate polarity, and they are fixed charges. The electrical field over the EOT is $E_{ox}=\pm 5$ MV/cm for $V_g>0$ and $V_g<0$, respectively. The sample used is the same as that in Fig. 1.

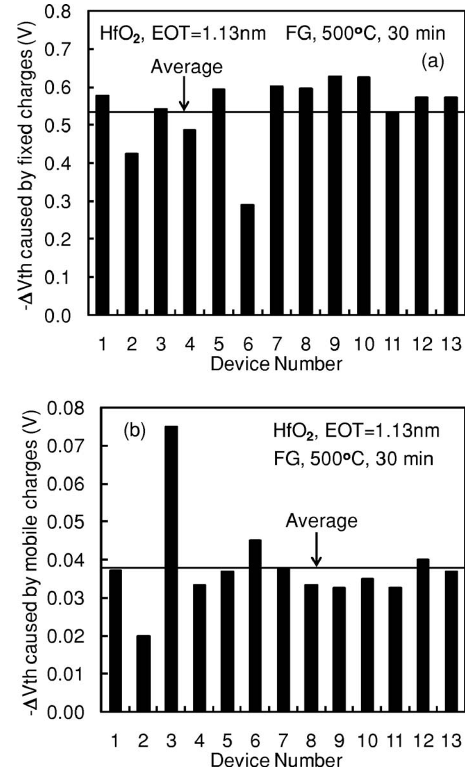

FIG. 7. Sample-to-sample variation of (a) process-induced FPC and (b) MPC. Thirteen *p*MOSFETs at random sites were subjected to the same thermal exposure in FG at 500 °C for 30 min. The fabrication of these samples is the same as that in Fig. 1.

D. Sample-to-sample variations

Figures 7(a) and 7(b) show that the FPC and MPC after 13 *p*MOSFETs were exposed to forming gas at 500 °C for 30 min. A large sample-to-sample variation exists in both of them. To confirm that this variation was induced by the thermal exposure, the preexposure sample-to-sample variation was checked. Figure 8(a) clearly shows that the variation is indeed caused by the exposure. Figure 8(b) shows that the sample-to-sample variation of SIPCs was negligible, when compared with that of PIPC. The different behavior of SIPC and PIPC indicates that they originate from different defects. The cause for the large sample-to-sample variation of PIPC is not known at present.

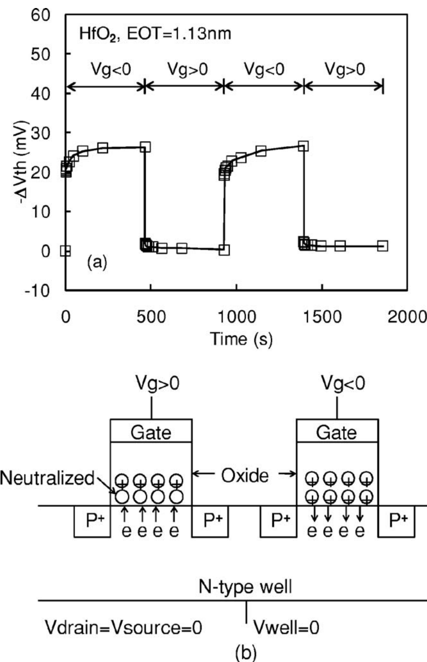

FIG. 6. Effects of gate bias polarity on the SIPC. Under $V_g>0$, the SIPC-induced $|\Delta V_{th}|$ is reduced, which is opposite to the PIPC-induced increase of $|\Delta V_{th}|$ in Fig. 5(a). In (b), it is illustrated that electron tunneling from the substrate neutralizes the SIPC under $V_g>0$. Unlike PIPC, the density of SIPC can be changed by V_g polarity. The electrical field over the EOT is $E_{ox}=\pm 5$ MV/cm for $V_g>0$ and $V_g<0$, respectively. The sample used is the same as that in Fig. 1.

IV. DEPENDENCE ON PROCESSING CONDITIONS

In this section, we will investigate how the PIPC depends on hydrogenation, gate material, conduction channel polarity, nitridation, source/drain activation, and replacing HfO_2 with Hf silicates.

A. Hf silicates

The results reported so far were obtained from HfO_2. Although Hf silicates have a lower dielectric constant than HfO_2, they increase the crystallization temperature of Hf-based oxide layers and improve process integration. It is important to find out if the addition of silicon to HfO_2 can eliminate PIPC. Figures 9(a) and 9(b) show that both FPC and MPC can also exist in Hf silicates. The average effective density of FPC is around 3×10^{12} cm^{-2}, which is significant.

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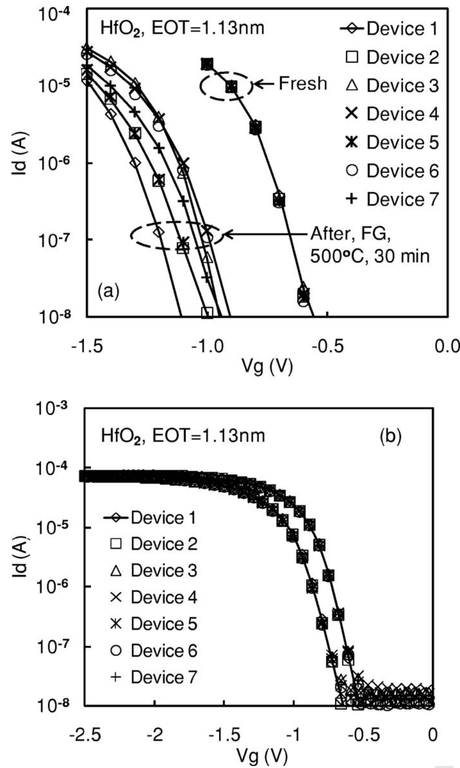

FIG. 8. (a) compares the sample-to-sample variation before and after PIPC formation. The sample-to-sample variation is negligible before PIPC formation. (b) shows that the sample-to-sample variation is also negligible for the SIPC. The sample used is the same as that in Fig. 1.

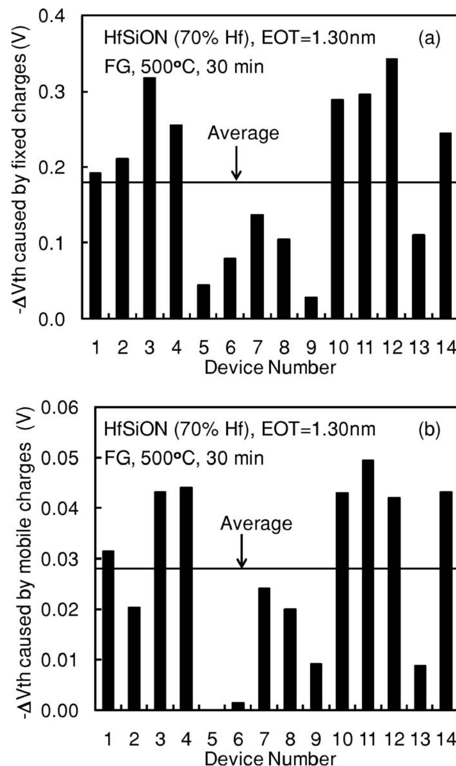

FIG. 9. (a) Process-induced fixed and (b) mobile positive charges in an Hf-silicate stack. The Hf silicate is 1 nm with 70% Hf, nitrided in NH_3 at 800 °C for 60 s. The EOT is 1.3 nm. The thermal exposure was in FG at 500 °C for 30 min. The devices are at random sites.

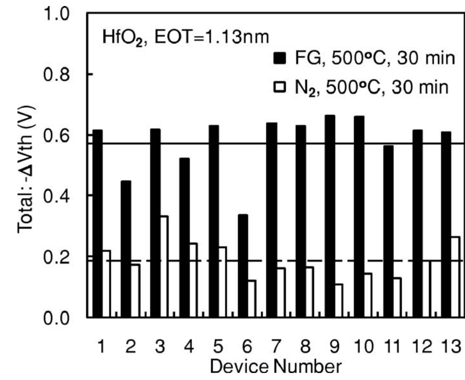

FIG. 10. A comparison of PIPC in FG with that in N_2. The exposure was at 500 °C for 30 min. The $|\Delta V_{th}|$ here is caused by the sum of fixed and mobile positive charges. The solid and dashed horizontal lines represent the average $|\Delta V_{th}|$ for FG and N_2, respectively, and $|\Delta V_{th}|$ in FG is clearly higher than that in N_2. The sample used is the same as that in Fig. 1. The devices are at random sites.

B. Hydrogenation

For SiO_2, it is concluded that the PIPC is hydrogen related.[12–16] Here, we will explore whether PIPC in Hf-based gate stacks is also hydrogen related. The thermal exposure of test samples was in FG so far, and Fig. 2 shows that PIPC is thermally activated. To study if hydrogen plays an active role, we compare the results after FG and N_2 exposure in Fig. 10. Despite the sample-to-sample variation, the average $|\Delta V_{th}|$ after FG exposure is clearly higher. To eliminate the sample-to-sample variation, a test was carried out by exposing a sample first in N_2 and then in FG at the same temperature. Figure 11 shows that the PIPC is higher after the FG exposure. This indicates that hydrogen is a reactant in the process of positive charging and the mobile positive charge can be a hydrogen-related species. It is likely that even the PIPC in N_2 was caused by hydrogenous species prestored in devices, which could be relocated during thermal exposure.

To support the above speculation, we monitored the transient transportation of MPC. It is well known that hydrogen movement through dielectric is dispersive,[24,25] rather than a first-order process.[4,8] Figure 12 confirms that MPC transportation does not follow the first-order kinetics and saturation

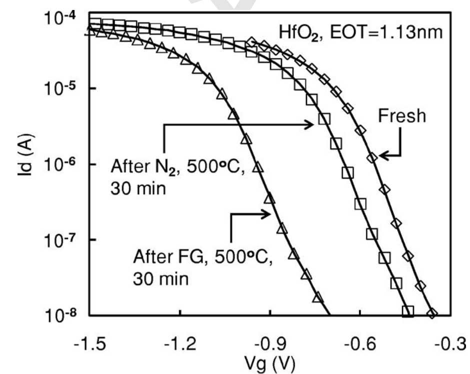

FIG. 11. A comparison of PIPC in FG with that in N_2 on the same device. The device was first exposed to N_2 at 500 °C for 30 min. After measuring the I_d-V_g (□), it was exposed to FG at 500 °C for a further 30 min. The positive charging is substantially higher when H_2 is present in the ambient. The sample used is the same as that in Fig. 1.

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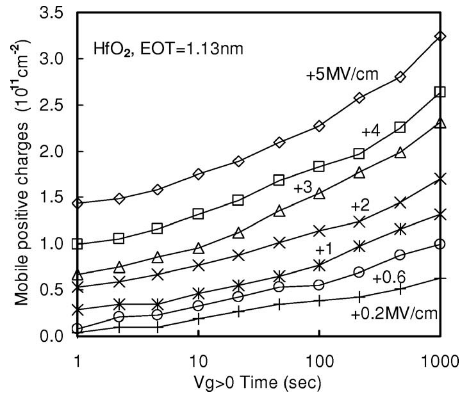


FIG. 12. Transportation of mobile positive charges under different oxide fields, E_{ox}(EOT). The movement is field enhanced. The kinetics does not follow the first-order reaction model and saturation is not observed. The exposure was in FG at 500 °C for 30 min. The sample used is the same as that in Fig. 1.

is not observed. A detailed study of MPC transportation in Hf-based gate stacks is out of the scope of this work.

Regarding how H_2 enters the gate dielectric stack, two possible routes are a vertical diffusion through the gate or a lateral diffusion through the gate edge. For SiO_2, it was reported that both H_2 (Ref. 26) and H_2O (Ref. 27) diffused laterally through the gate edge, since an increase of channel length, L, led to a reduction of defects per unit gate area. In principle, the dependence of PIPC on L could also give an indication of the route of H_2 diffusion into Hf-based gate stacks. However, we could not obtain clear results and conclusion because the large variation of PIPC for devices of the same size (see Sec. III D) drowned the effect of L.

C. Absence of process-induced positive charges

As mentioned in the Introduction, positive charging by H_2 exposure at 500 °C is absent in a device-grade SiO_2 film. The question is if PIPC can also be suppressed in Hf-based gate stacks. Figure 13 shows that this is the case. Differences between the samples used in Figs. 13 and 1 exist in gate material, conduction channel polarity, and nitridation. They will be studied one by one below.

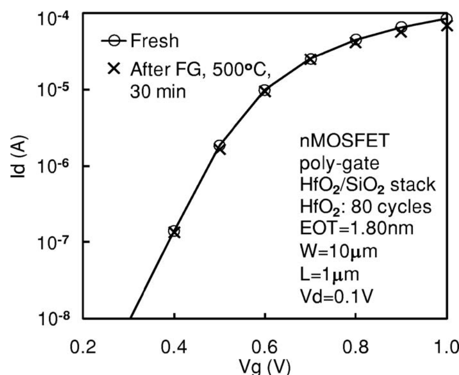
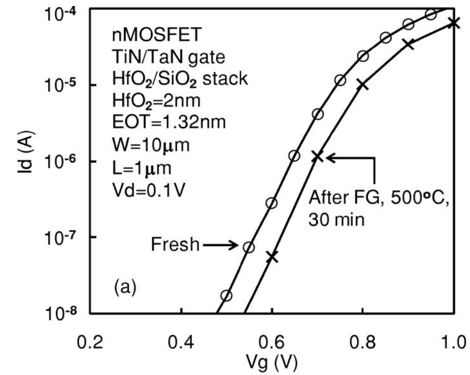


FIG. 13. Absence of PIPCs in an Hf stack. The *n*MOSFET has a 4 nm HfO_2 and an n^+ poly-Si gate. Nitridation was not performed for this batch. The thermal exposure was in FG at 500 °C for 30 min.



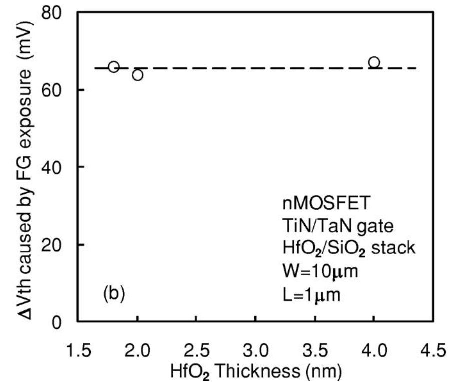


FIG. 14. (a) Impact of gate materials on PIPC. The *n*MOSFET has a TaN gate and a 2 nm HfO_2 that was not nitrided. PIPC can also be negligible for *n*MOSFETs of a TaN gate. (b) shows that the positive shift of the $I_d - V_g$ in (a) was independent of HfO_2 thickness, indicating that it originates from a change in the work function of gate metal.

D. Gate material

The gate is n^+ poly-Si in Fig. 13 and TaN in Fig. 1. In the early days of CMOS technologies, it was reported that gate material played an active role in PIPC.[28,29] To find out if the PIPC in Fig. 1 is caused by the use of TaN gate, we used TaN-gated *n*MOSFETs in Fig. 14(a). It is clear that PIPC can also be absent in TaN-gated samples.

Figure 14(a) shows that there is a positive shift of $I_d - V_g$, and this should be explained. Two potential sources for the positive shift are negative charging[30] and an increase of the work function of TaN.[23] These two can be separated by examining ΔV_{th} dependence on HfO_2 thickness. The charging-induced $|\Delta V_{th}|$ always increases with the thickness of HfO_2,[31] while the work function change will give a thickness-independent $|\Delta V_{th}|$. Figure 14(b) supports that the increase of TaN work function is responsible for the positive shift in Fig. 14(a). This increase in TaN work function is also in agreement with the increase observed for TaN deposited on SiO_2.[23]

E. Conduction channel polarity

For SiO_2, it was reported that PIPC can occur in *p*MOSFETs, but not in *n*MOSFETs on the same wafer.[16] It is also proposed that the hole density at the interface can play a role in positive charging.[32] Figure 1 shows that PIPC occurs in *p*MOSFETs and Figs. 14(a) show that it does not occur in *n*MOSFETs. However, these *p*MOSFETs and *n*MOSFETs were fabricated on different wafers and in different batches.

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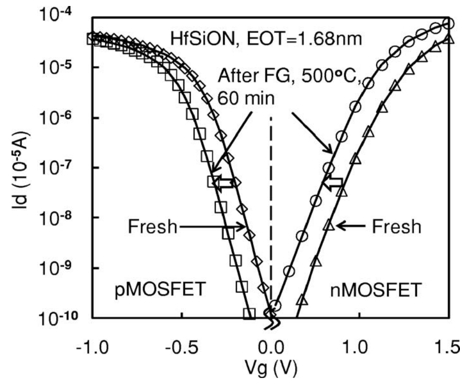

FIG. 15. A comparison of PIPC in a *p*MOSFET and an *n*MOSFET fabricated on the same wafer. The PIPC is insensitive to conduction channel polarity. The Hf silicate is 3 nm with 80% Hf and plasma nitrided. The exposure was in FG at 500 °C for 60 min.

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297 To have a direct comparison, Fig. 15 presents PIPC in 298 *n*MOSFETs and *p*MOSFETs fabricated on the same wafer. It 299 is obvious that PIPC is insensitive to conduction channel 300 polarity.

301 F. Nitridation

302 The Hf-based gate stacks for both Figs. 13 and 14 were 303 not nitrided, but were nitrided in NH_3 for the samples used in 304 Figs. 1–12. We found that PIPC was substantial 305 ($>10^{12}$ cm^{-2}) in all three batches of tested samples nitrided 306 in NH_3. Figure 15 shows that PIPC also exists in a plasma-307 nitrided Hf-based gate stack. We conclude that nitridation 308 enhances PIPC. However, we will show next that PIPC can 309 also be formed in an Hf-based gate stack without nitridation.

310 G. Activation anneal

311 For PIPC in SiO_2, nitridation is not essential.[12–16] Figure 312 16 shows that substantial PIPC can also occur in an Hf-based 313 gate stack without nitridation. Here, the source and drain 314 were activated by solid phase epitaxial regrowth at 650 °C 315 for 1 min, while the activation was by a 1000 °C spike in the 316 rest of the Hf samples. For SiO_2 prepared at low temperature, 317 it was reported that its quality was generally inferior.[33] It 318 appears that the lack of the 1000 °C process step also leads 319 to poor quality Hf-based gate stacks and serves to enhance 320 PIPC.

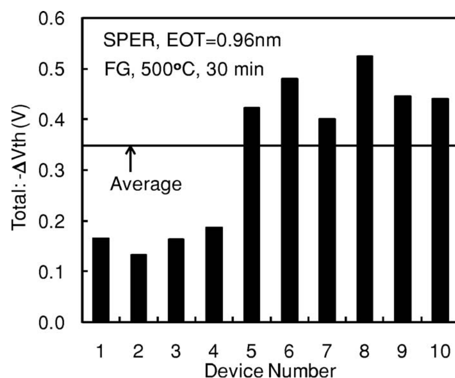

FIG. 16. PIPC in Hf layers without nitridation. *n*MOSFETs have a 2 nm HfO_2 and a TaN gate. Unlike the other samples used in this work, the source and drain were activated by solid phase epitaxial regrowth at 650 °C for 60 s. The exposure was in FG at 500 °C for 30 min. The devices are at random sites.

V. CONCLUSIONS 321

Process-induced positive charging (PIPC) in Hf-based 322 gate stacks was investigated in this work. It is found that a 323 substantial amount of PIPC ($10^{12}-10^{13}$ cm^{-2}) can be formed 324 after a 500 °C exposure to forming gas for 30 min. They 325 originate from charges in the gate dielectric rather than in-326 terface states. Unlike the stress-induced positive charge 327 (SIPC), once formed, PIPC is not neutralized under $V_g>0$ or 328 at elevated temperature. PIPC has two components: mobile 329 and fixed positive charges. The mobile charges can be moved 330 within Hf stacks, but their number will not change. Both 331 mobile and fixed charges exhibit a large sample-to-sample 332 variation, although this variation is negligible for fresh and 333 electrically stressed samples. 334

The dependence of PIPC on process conditions is exam-335 ined. PIPC occurs in both HfO_2 and Hf silicates. It is higher 336 when H_2 is present in the ambient during the thermal expo-337 sure, indicating hydrogen plays an active role. PIPC is insen-338 sitive to both gate material and conduction channel polarity. 339 However, nitridation significantly enhances PIPC. Without 340 nitridation, PIPC is negligible in the sample that went 341 through a 1000 °C spike activation, but still exists in 342 samples where the activation was at 650 °C through solid 343 phase epitaxial regrowth. 344

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