Stress-Induced Positive Charge in Hf-Based Gate Dielectrics: Impact on Device Performance and a Framework for the Defect

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***Abstract*—A Hf-based dielectric has been selected to replace SiON for CMOS technologies. When compared with SiON, Hf dielectrics can suffer from higher instability. Previous attentions were focused on electron trapping, and positive charging received less attention. The objective of this paper is to study the impact of positive charging on device performance and to provide a framework for the defect. Three components of threshold voltage instability ΔVth are unambiguously identified for pMOSFETs, i.e., loop, loop-shift, and up-loop. The loop dominates ΔVth at a relatively short time (< 1 s). After stressing for a longer time, the whole loop is shifted in the negative direction. Unlike the loop, the up-loop cannot readily be recharged after recovery. In addition to the generated interface states, three different types of positive charges are formed in the Hf-based stacks, i.e., cyclic positive charges (CPC), antineutralization positive charges (ANPC), and as-grown hole trapping (AHT). Each type of defect has its unique signatures and properties. CPC can repeatedly be charged and discharged by alternating the gate bias polarity. ANPC is more difficult to neutralize, whereas AHT is harder to charge. Both the generated interface states and the AHT saturate at longer stress time, but ANPC does not. ANPC reduces at higher measurement temperature, but CPC is insensitive to temperature. The relation between each type of defect and each component of ΔVth is clarified.**

***Index Terms*—Degradation, gate stacks, HfO_2, hf-silicates, negative bias temperature instability (NBTI), positive charges, traps.**

I. Introduction

As THE thickness of silicon oxynitrides approaches 1 nm, the gate leakage current becomes intolerable. To keep the downscaling of MOSFETs on track of Moore's law, there is a pressing need for replacing SiON by a gate dielectric of higher dielectric constant (high-k). This has motivated a worldwide research in high-k layers since 1990s [1]–[5]. After investigating many different materials, the Hf-based dielectrics have been selected as the gate dielectric for CMOS technologies. When compared with SiON, Hf dielectrics suffer from lower carrier mobility and higher instability [1]–[5].

On the instability, both electron trapping [3]–[6] and positive charging [7]–[11] in Hf-based dielectrics have been reported. The electron trapping is highly dynamic [5], [6], [12] and rapidly reduces as the Hf dielectrics become thinner [4], [13], [14]. When compared with electron trapping, the stress-induced positive charging received relatively less attention. Positive charging is rarely observed for nMOSFETs due to the masking effects of electron trapping [9]–[11], although it contributes to the negative bias temperature instability (NBTI) of pMOSFETs [7]–[10]. For sub-2-nm Hf dielectric, we will show that positive charging can lead to larger Vth instability for pMOSFETs than the electron trapping-induced instability of nMOSFETs. Despite its importance, our understanding of the positive charging is poor. Its impact on device performance is not fully understood, and there is little information on the defect. The objective of this paper is to address these issues and to provide a framework for the defect.

We will report clear results, showing that the instability in threshold voltage ΔVth of pMOSFETs has three components. The first one appears as a "loop" in the two transfer characteristics (TCs) measured during the rising and falling edges of a gate voltage pulse, similar to the Vth instability observed for nMOSFETs [1], [5], [6], [12]. It dominates the instability at short time (< 1 s). The second is a shift of the whole loop, and the third is an up-loop, which counts for the difference between the total ΔVth and the sum of the loop and loop-shift.

On the defect, historically, positive charging in SiO_2 has puzzled the international community for decades. Some positive charges behave so strangely that they are called by various names, such as anomalous positive charges [15], slow states [16], and border traps [17]. It has recently been reported that the anomalous behavior originates from the simultaneous presence of different types of positive charges in SiO_2, i.e., cyclic positive charge (CPC), antineutralization positive charge (ANPC), and as-grown hole trapping (AHT) [18]–[20]. For Hf-based dielectrics, there are two questions. One is whether the same types

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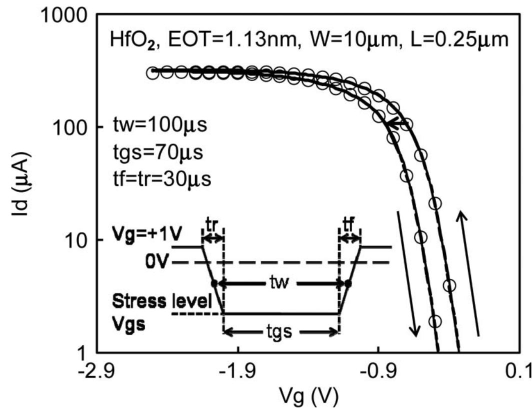

Fig. 1. TCs corresponding to the two edges of a gate bias pulse shown in the inset. The rising and falling time is 30 μs, and the peak time is 70 μs, giving a pulse width of 100 μs. The negative shift of the falling TC from the rising TC indicates positive charge formation. The solid lines represent the TCs when the gate pulse was applied to a fresh device. The dashed lines represent the TCs when the same pulse was applied again. The symbol "o" represents the TCs obtained by applying quasi-dc Vg ramps, where Vg was ramped from +1 to −2.5 V in 4 s and then back to +1 V.

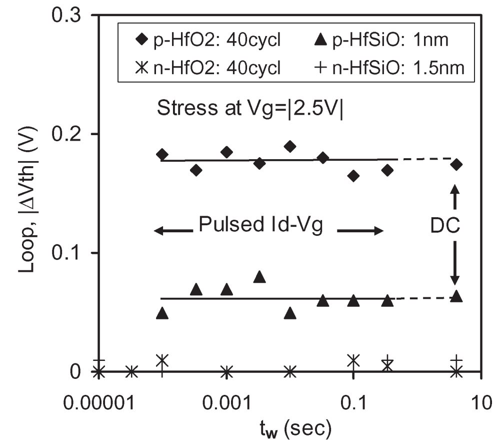

Fig. 2. Dependence of loop size $|\Delta\text{Vth}|$ on the gate pulse width tw. The measurement time is proportional to tw, and the $|\Delta\text{Vth}|$ is clearly insensitive to tw. The quasi-dc measurement was obtained by applying two voltage ramps, and the ramp time is 4 s. The instability of pMOSFETs can substantially be higher than that of nMOSFETs for sub-2-nm Hf dielectrics.

of defects also exist. If this is true, the other question is what is the relation between each type of defect and the three components of ΔVth. These questions will be answered in this paper.

II. Devices and Experiments

A. Devices

For a 3-nm or thicker Hf layer, electron trapping and positive charging can simultaneously occur [9], [10]. This is highly undesirable for studying positive charges, since electron trapping compensates positive charging and complicates the analysis. To simplify the test condition, electron trapping should be suppressed. Recent work [4], [13] shows that electron trapping is substantially suppressed in 2-nm or thinner Hf layers. As a result, 2-nm or thinner Hf layers are selected as test samples in this paper.

Both HfO_2 and Hf-silicate were prepared by atomic layer deposition. Before depositing HfO_2, the chemical SiO_2 was nitrided in NH_3 at 900 °C for 60 s. A 2-nm HfO_2 was then prepared, resulting in an equivalent oxide thickness (EOT) of 1.13 nm. For the Hf-silicate, a 1-nm HfSiO (70% Hf) layer was deposited and then nitrided in NH_3 at 800 °C for 60 s, giving an EOT of 1.3 nm. A 1000 °C spike was used to activate the source and drain dopant, and the gate is TaN. The channel length and width of pMOSFETs is 0.25–1 and 10 μm, respectively.

To facilitate the comparison, nMOSFETs were also prepared with 2-nm HfO_2. The gate metal, channel length, and width are the same as those of pMOSFETs. A 5.5-nm SiO_2 and a 2.7-nm SiON were also used for comparison.

B. Experiments

Both the pulsed Id∼Vg [5], [6], [12] and the traditional quasi-dc Id∼Vg [21], [22] were used to monitor the positive charge. The waveform of the gate pulse used is given in the inset of Fig. 1. The gate bias was ramped from +1 V to a stress level of Vgs and stayed at Vgs for a time of tgs before being ramped back to +1 V in a time of tf. "tw" is the pulse width. For the quasi-dc Id∼Vg, the ramp time is 4 s, and the tgs is 0.15 s. As shown in Fig. 1, the shift of the threshold voltage ΔVth is assessed at a fixed drain current of 10^{-5} A with a drain bias of −0.1 V for both pulse and quasi-dc tests. The positive charge in the Hf stack is evaluated from the shift of gate voltage at midband of silicon [23], [24]. Since the distribution of positive charge within the Hf stack is not known, we follow the well-accepted practice and use the "effective charge density" ΔNot by assuming the charge centroid being at the oxide/substrate interface [23], [24]. The generated interface states were assessed from the change in the subthreshold swing [24], [25]. The stress of the Hf dielectric was carried out under a constant gate bias with all the other terminals grounded. For SiO_2, the substrate hole injection (SHI) [18]–[20] was also used to stress the device. The range of temperature is 25 °C to 200 °C. In some tests, the stress and measurement temperature was kept the same, but there were also tests where they were different. When ΔVth was evaluated, the stressed and reference Id∼Vg were always measured at the same temperature. Further details of the measurement techniques can be found from earlier works [5], [6], [12], [18], [21], [22].

III. Impact on Device Performance

In this section, we will show that the positive charging-induced ΔVth has three components, i.e., loop, loop-shift, and up-loop.

A. Loop

Fig. 1 shows the Id∼Vg corresponding to the rising and falling edge of a gate voltage pulse given in the inset. When Id fell, it did not follow the same curve as when Id rose. Id∼Vg is moved in the negative direction, and a "loop" is formed, indicating positive charge formation. When the same pulse was applied again, the dashed lines in Fig. 1 show that the same loop was obtained.

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Fig. 2 plots the loop size ΔVth against the pulse width (tw), and the measurement time is proportional to tw. It clearly shows that the ΔVth observed here is insensitive to the measurement time in a range from tens of microseconds to seconds. The data marked by "DC" was obtained by using quasi-dc Vg ramps with a ramp time of 4 s. To further illustrate the insensitivity of ΔVth to measurement time, the quasi-dc Id∼Vg is given in Fig. 1 as the symbol "o" and it agrees well with the pulsed Id∼Vg. This is in contrast with the substantial reduction of |ΔVth| when measured by quasi-dc Id∼Vg for both Hf-based nMOSFETs [5], [6], [12], [13] and the pMOSFETs with a SiON gate dielectric [24], [26], [27]. An explanation will be given when we address the defect responsible for the loop in Section IV-C.

The ΔVth of nMOSFETs and pMOSFETs with the same HfO_2 thickness is compared in Fig. 2. It clearly shows that the Vth instability of pMOSFETs can be higher. The insignificant |ΔVth| for nMOSFETs in a sub-2-nm Hf layer agrees with early works [4], [13]. This confirms that any compensation of electron trapping on positive charging is negligible in this paper.

B. Loop-Shift

When the stress time is shorter than 1 s, Fig. 3(a) shows that the loop dominates ΔVth and does not increase with stress time. This is in contrast with the typical NBTI, where the instability increases [28], [29]. For longer stress, ΔVth does increase, but we will show the loop remaining the same.

The gate bias waveform used is given in Fig. 3(b). Initially, two voltage ramps labeled as "A" and "B" were applied, and the corresponding Id∼Vg in Fig. 3(c) shows the expected loop. After stressing the device at Vgs $= -2.5$ V for 2×10^4 s, three voltage ramps ["C," "D," and "E" in Fig. 3(b)] were applied, and the resultant Id∼Vg is labeled as "C," "D," and "E" in Fig. 3(c). Several observations can be made. First, when Vg was ramped from the stress level toward positive after the long stress (ramp "C"), Id∼Vg was shifted further negatively from "B" to "C," confirming more positive charging during the stress. Second, when Vg was ramped from $+1$ V in the negative direction (ramp "D"), the difference between "C" and "D" in Fig. 3(c) shows a loss of positive charges, typically referred to as "recovery" [24], [30]. Third, when Vg was ramped toward positive again (ramp "E"), the curve "E" appears between "C" and "D." The difference between "E" and "C" will be addressed in the next section, and here, we explore the relation of the four Id∼Vg: "A," "B," "D," and "E."

Since the ramps "D" and "E" in Fig. 3(b) are the same as the "A" and "B" used to measure the loop, the negative shift from "D" to "E" shows that the loop still exists after the long stress. Furthermore, the difference between "E" and "D," "E"–"D," is the same as "B"–"A," so the loop size is unchanged before and after stress. This indicates that the defects responsible for the loop are cyclic, and their density is not affected by the charging and discharging during the test. However, the stress negatively shifted the whole loop, and the loop-shift can be evaluated either from the two rising Id–Vg ("D"–"A") or the two falling Id–Vg ("E"–"B"). If the loop-shift is recoverable, one would expect |"E"–"B"| > |"D"–"A"|, since "E" was measured after recharging at Vg $= -2.5$ V. The fact that |"E"–"B"| = |"D"–"A"| indicates that the loop-shift recovery is negligible. Since the loop-shift has no influence on the loop size, the loop and the loop-shift must originate from different types of defect, which will be further investigated in Section IV. Fig. 3(c) was obtained after a stress time of

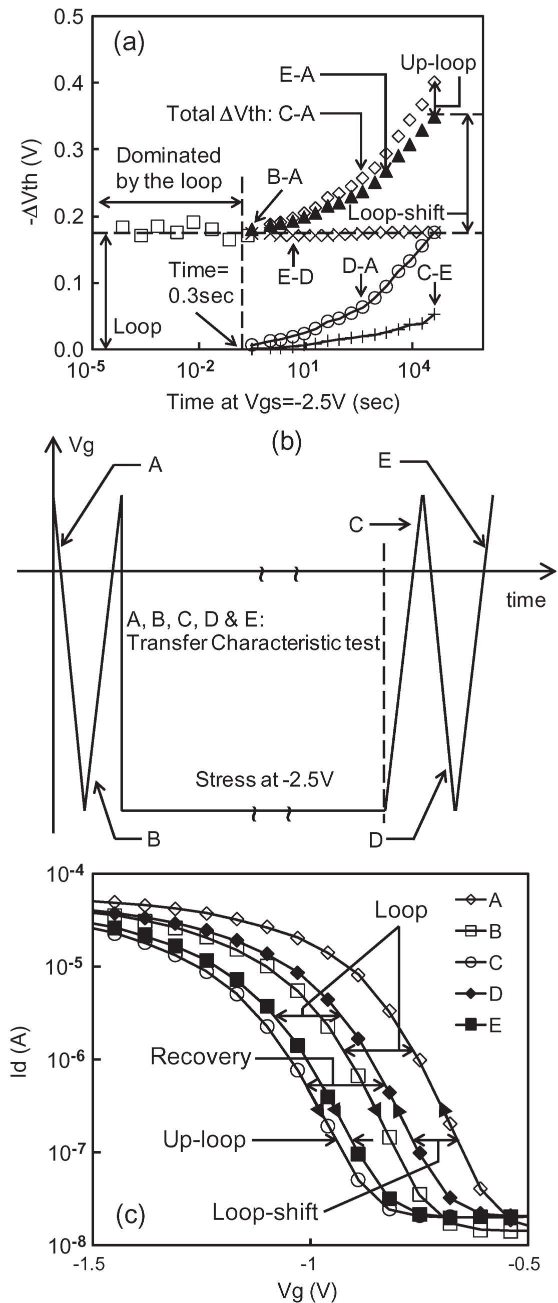

Fig. 3. Separation of three components of Vth instabilities: loop, loop-shift, and up-loop. (a) Instability was dominated by the loop at short time, and the loop is insensitive to stress time. The symbol □ was obtained from the pulsed Id∼Vg shift. For stress time longer than 0.3 s, the data in (a) were obtained by applying the gate bias given in (b). Here, two Vg ramps labeled "A" and "B" were first applied, and the corresponding Id∼Vg is shown as the curve "A" and "B" in (c). After stressing at Vgs $= -2.5$ V for a prespecified time, three further Vg ramps labeled as "C," "D," and "E" were applied. As an example, the three Id∼Vg after a stress time of 2×10^4 s are shown as the curve "C," "D," and "E" in (c). The symbol ▲ in (a) is the sum of the loop (×) and the loop-shift ("o"). The symbol ◇ in (a) is the total Vth instability, the sum of the loop (×), the loop-shift ("o"), and the up-loop (+).

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2×10^4 s. Fig. 3(a) shows the evolution from a fresh device to Fig. 3(c). The loop size clearly remains the same during the stress, but both the loop-shift and the up-loop increase with stress time.

C. Up-Loop

The traditional NBTI is the total ΔVth, namely, "C"–"A" in Fig. 3(c), and it can be divided into

$$\Delta\mathrm{Vth}(\text{`C'} - \text{`A'}, \mathrm{Total}) = \Delta\mathrm{Vth}(\text{`D'} - \text{`A'}, \text{loop-shift}) + \Delta\mathrm{Vth}(\text{`C'} - \text{`D'}, \mathrm{Recovery}).$$

As described earlier, the loop-shift does not recover. The recoverable part consists of two components

$$\Delta\mathrm{Vth}(\text{`C'} - \text{`D'}, \mathrm{Recovery}) = \Delta\mathrm{Vth}(\text{`E'} - \text{`D'}, \mathrm{Loop}) + \Delta\mathrm{Vth}(\text{`C'} - \text{`E'}, \text{Up-loop}).$$

To find out the difference between these two, we reexamine Fig. 1. When the same gate pulse was applied twice, the same rising and falling Id∼Vg were obtained. The good agreement for the two rising Id∼Vg indicates that the application of Vg = +1 V at the end of the first pulse led to a full neutralization of relevant defect, and consequently, the loop is recoverable. The good agreement for the two falling Id∼Vg means that the defects responsible for the loop were fully recharged during the second pulse. This is in contrast with Fig. 3(c), where the difference between "C" and "E" indicates that some defects were not recharged by reapplying a Vg ramp after neutralization. This component "C"–"E" will be referred to as "up-loop" hereafter. The stress time is less than 1 s for Fig. 1 and 2×10^4 s for Fig. 3(c). Fig. 3(a) shows that the up-loop ("C"–"E") is negligible at short time (< 1 s) and builds up as the stress time increases. In Section IV, more results will be presented to support that the loop and up-loop originate from different defects.

IV. Framework for Defects

A. Types of Positive Charge in SiO_2

To have a benchmark for positive charge in Hf stacks, a brief review of the positive charge in SiO_2 will be given. A typical and summarizing result reported for SiO_2 is reproduced in Fig. 4(a) [18]. Here, positive charges were first formed during SHI with an oxide field of Eox = −5 MV/cm. A Fowler–Nordheim electron injection was then used to neutralize them. This is followed by alternatively applying Vg < 0 and Vg > 0 with Eox = ±5 MV/cm. Under Vg < 0, some of the neutralized positive charge can be recharged without resuming hole injection. When the gate bias polarity is switched, part of the positive charge can repeatedly be neutralized and recharged, so that they are called as CPC. The neutralization of some positive charge under Vg > 0 is more difficult than their charging under Vg < 0, and they are referred to as ANPC.

Fig. 4(b) and (c) shows that the energy level of ANPC is higher than that of CPC and is above the bottom edge of the Si conduction band. This explains the difficulty in neutralizing ANPC. Under the same Eox = −5 MV/cm, the recharging

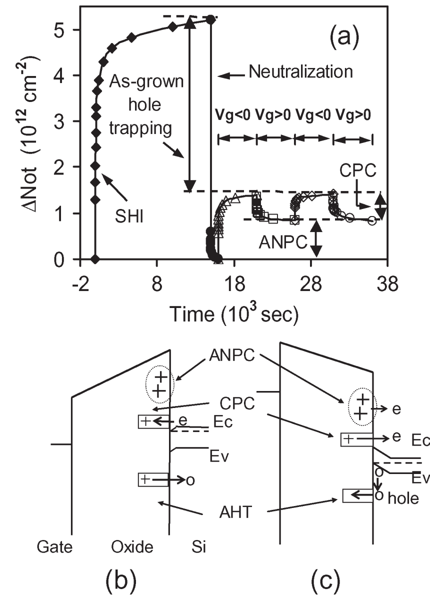

Fig. 4. Presence of three different types of positive charges in a 5.5-nm SiO_2. (a) Test sequence. Initially, positive charging built up during an SHI under an oxide field of Eox = −5 MV/cm, an n-well and p-substrate bias of 6 and 7 V, respectively [18]. The neutralization was under Eox = +8 MV/cm. This was followed by alternately applying Vg < 0 (Eox = −5 MV/cm) and Vg > 0 (Eox = +5 MV/cm), with all the other terminals grounded. The (b) neutralization and (c) charging of CPC only involve electron tunneling at the same energy level. The ANPC has an energy level above the conduction band edge of Si, making its neutralization difficult. For the same Eox = −5 MV/cm, the charging level without switching on SHI is well short of that with SHI, since AHT cannot be filled by holes near the top edge of the Si valence band (c).

under Vg < 0 without SHI clearly did not reach the level when SHI was switched on. This indicates that some defects are difficult to recharge without accelerating holes in the substrate, as illustrated in Fig. 4(c), and they are AHT [18]–[21].

Eox = ±5 MV/cm was selected here for the cycled test. An increase of |Eox| will result in a higher CPC. However, the AHT does not depend on this Eox so long as the same Eox is used for sensing during the stress and cycled tests, since the CPC charge is subtracted out when AHT is evaluated, as shown in Fig. 4(a). ANPC does not depend on this Eox either, if the magnitude of Eox < 0 and Eox > 0 is kept the same. The cyclic nature of CPC means that it is neutralized at the end of Eox > 0 period, where ANPC is assessed in Fig. 4(a). More details on how to separate AHT from CPC and ANPC and their different properties can be found in our early works [18]–[21].

B. Types of Positive Charge in Hf-Based Dielectrics

For SiO_2 or SiON, the three types of positive charge were insensitive to either stress or process conditions [18], [24]. For example, Fig. 4(a) was obtained after stressing a 5.5-nm SiO_2 by SHI [18]. The same three types of positive charge were also observed in a 2.7-nm SiON layer after negative bias temperature stress [24]. The question is whether the same types of positive charge can be formed in Hf stacks.

Fig. 5(a) and (b) shows the behavior of positive charges in pMOSFETs with HfO_2 and HfSiON, respectively. The devices were first stressed under Vg < 0, and the positive charge built up. Following a neutralization step, the gate bias polarity was

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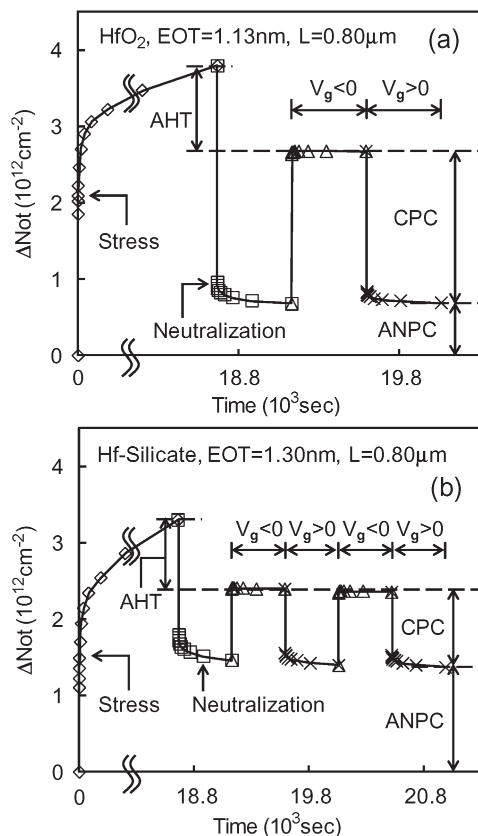

Fig. 5. Types of positive charges in (a) HfO_2 and (b) Hf-silicate (70% Hf). The HfO_2 and Hf-silicate was first stressed for a relatively long time (18 662 s) under Vg $= -2.5$ and -2.8 V, respectively. The stress period is not drawn to scale here. To determine the types of positive charges, the sensing phase started with the neutralization carried out under $\mathrm{Eox(EOT)} = +6.5$ MV/cm, followed by applying Vg < 0 and Vg > 0 corresponding to $\mathrm{Eox(EOT)} = \pm 5$ MV/cm, respectively. A comparison with Fig. 4(a) indicates that the same three types of positive charges were formed in SiO_2 and Hf-dielectrics.

alternated, and the magnitude of electrical field across the interfacial layer was kept at 5 MV/cm. The first impression is that the positive charge in both HfO_2 and HfSiON behaves remarkably similar to that in SiO_2, suggesting that the same types of positive charge were formed. Further evidences supporting this statement will be given in the following sections.

A comparison of the curve labeled as "neutralization" for SiO_2 in Fig. 4(a) with that for the Hf-based stacks in Fig. 5(a) and (b) shows that the positive charge was only fully neutralized in the former case. This difference is not fully understood at present. There are two possible reasons, i.e., the inclusion of the high-k layer and the reduction in layer thickness. Fig. 4 used a 5.5-nm SiO_2 and Fig. 5(a) used a 2-nm HfO_2 with an EOT of 1.13 nm. If the reduction of thickness is responsible for the difference, one would expect a similar difference if a thinner SiO_2 or SiON is used. Our results [24] confirm that the neutralization was also incomplete for a 2.7-nm SiON film. We speculate that a thinner layer could raise the energy level of ANPC, making its neutralization difficult.

Finally, we would like to point out that, although the Hf stacks used in this paper were nitrided, the same three types of positive charges were observed for Hf stacks without nitridation (not shown). Nitridation does not introduce a new type of positive charges. Although the density of positive charges

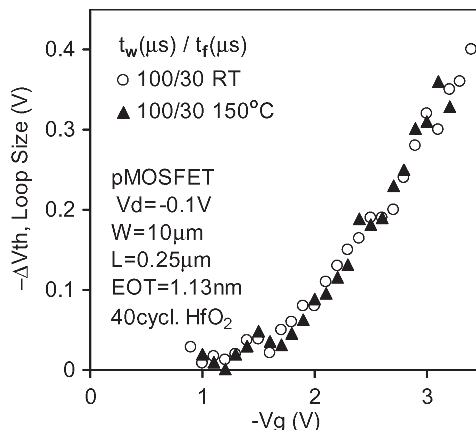

Fig. 6. Dependence of the loop on temperature. In this test, the stress and measurement were at the same temperature. The loop is clearly insensitive to temperature.

depends on process conditions [18], [24], [31], the framework proposed here for positive charges is not process specific. In the following, we will study which type of defect is responsible for each component of ΔVth reported in Section III.

C. Defect for the Loop

As described earlier, the same loop in Fig. 1 was obtained when a gate pulse was applied twice, indicating that the defect can repeatedly be positively charged under Vg < 0 and neutralized under Vg ≥ 0. This suggests that the loop originates from CPC, since all the other types of defects are not cyclic. A key test for this suggestion will be the loop's dependence on measurement temperature. As illustrated in Fig. 4(b) and (c), the charging and discharging of CPC only involves carrier tunneling at the same energy level. Since tunneling is insensitive to temperature, CPC is insensitive to temperature too, which is confirmed by our early work [18], [24]. If the loop originates from CPC, it must be insensitive to temperature. This is confirmed in Fig. 6. As a result, the loop has all the features of CPC, strongly supporting that it originates from CPC.

To assess the contribution of the generated interface states ΔDit to the loop, we will use both the Id∼Vg of pMOSFETs and the high-frequency capacitance–voltage (CV) characteristics measured on capacitors with an n-type substrate. Id∼Vg and C–V allow the assessment of ΔDit in the lower and up half of the silicon bandgap, respectively. Fig. 7 shows C–V when Vg was ramped from $+1$ V to -2.5 V and then back, which is the typical Vg ramp used for measuring the loop. There is little distortion in the C–V slope, so that ΔDit is negligible in the up half of the bandgap during loop measurement. A loop cannot be seen in the two C–Vs since the rise of capacitance occurs when Vg > 0. As mentioned earlier, CPC is neutralized under Vg > 0 and, consequently, has no effect on C–V. An inspection of Fig. 1 shows that the rising and falling Id∼Vg is in parallel within the subthreshold region. The ΔDit extracted from the subthreshold swing is given in Fig. 8, confirming that ΔDit is also negligible in the lower half of the bandgap when the loop dominates ΔVth.

We now speculate why the loop size ΔVth of the Hf-based pMOSFETs is insensitive to measurement time, unlike

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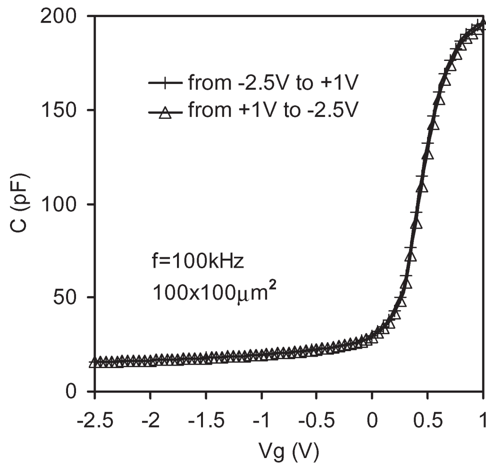

Fig. 7. Capacitance–gate voltage (C–V) characteristics of a MOS capacitor. For a fresh HfO_2 layer, the Vg was ramped from $+1$ V to -2.5 V and then back, which was typically used to measure the loop for a pMOSFET. The good agreement in the two C–Vs indicates that the creation of interface states in the up-half of the silicon bandgap during the measurement is negligible and contributes little to the loop.

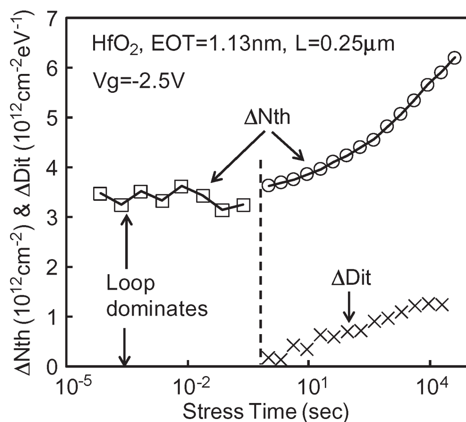

Fig. 8. Contribution of generated interface states ΔDit to the threshold voltage instability ΔVth. ΔNth = |ΔVth| × Cox/q, where Cox is the oxide capacitance per unit area, and q is one electron charge. ΔNth is the effective density of total charges by assuming all charges being at the dielectric/substrate interface. ΔDit is negligible when loop dominates but considerable at longer stress time. The test procedure is the same as that in Fig. 3.

Hf-based nMOSFETs and SiON-based pMOSFETs. The dominance of CPC for Hf-based pMOSFETs can throw some light on the difference. Fig. 4(b) shows that the neutralization of CPC requires a supply of free electrons from the substrate. For pMOSFETs, ΔVth is measured under Vg < 0, and free electrons are repelled from the dielectric/Si interface. This lack of free electrons at the interface weakens the neutralization of CPC and could be responsible for the insensitivity of CPC to measurement time. For Hf-based nMOSFETs, electrons can be detrapped by tunneling away from the defects, and a supply of carriers is not needed. For SiON-based pMOSFETs, ΔVth at short time is dominated by AHT [24], [26], [32]. Fig. 4(b) shows that the neutralization of AHT requires electrons tunneling from the Si valence band, namely, a hole tunneling away from AHT. Unlike free electrons needed for neutralizing CPC, there are plenty of valence electrons for neutralizing AHT even under Vg < 0 during the measurement, resulting in higher charge losses for longer measurement time.

Finally, it should be pointed out that the insensitivity of the loop to stress time in Figs. 2 and 3 indicates that CPC can preexist in the Hf stacks, whereas early works show that CPC is generated for SiO_2 [18]–[20] and SiON [24]. In this sense, the Hf stacks behave like a stressed SiO_2.

D. Defect for the Up-Loop

Since CPC is responsible for the loop, we effectively rule out that CPC can contribute to the other two components. This is because the loop and CPC do not increase with stress, but the others do. We now explore which defect is responsible for the up-loop.

Fig. 3(c) shows that both the loop and the up-loop lose their charge when Vg was ramped from the negative stress bias to $+1$ V. Unlike the loop, the up-loop was not recharged as Vg ramped back to the stress level. This means that the neutralization of the defect is much easier than its charging. An examination of Figs. 4 and 5 indicates that AHT is the only type of defect of such a property and must be responsible for the up-loop. Fig. 4(c) shows that both CPC and ANPC can positively be charged through electron tunneling away from them without involving hot holes, but this does not apply to AHT [18]–[21]. The energy level of AHT is below the top edge of the silicon valence band [33], [34], and AHT cannot be filled by holes at the top edge. Holes must be excited to be able to fill AHT. Since the hole density exponentially reduces away from the top edge, filling AHT is considerably more difficult than charging CPC and ANPC. This explains why the AHT was not recharged by applying a Vg ramp in Fig. 3(c). It also agrees with Fig. 1, where the application of a gate pulse twice does not produce any up-loop, since the pulse width (100 μs) is too short to fill AHT.

To further support that the "AHT" labeled in Fig. 5 is indeed the as-grown hole trap, we next examine its features. Early works [18]–[21] show that AHT should have the following characters: 1) the charging should be negligible at the start of the stress when traps are empty; 2) the charging must saturate as all traps are filled for sufficiently long stress time; and 3) the saturation level should be independent of stress conditions. If the "AHT" in Fig. 5 originates from the as-grown hole trap, it should possess all these characters.

Fig. 5 shows how AHT was assessed. A relatively long stress (18 662 s) was first used to charge the AHT. Both AHT and CPC were then neutralized. This was followed by applying Vg < 0 to recharge CPC, but not AHT, allowing their separation. Fig. 9 shows that AHT is negligible at short stress time, and it indeed saturates at longer time, and the saturation level is not sensitive to stress temperature. We found that the saturation was not sensitive to stress bias either (not shown). As a result, AHT has the expected characters of AHT.

The saturation level of AHT in the Hf stack is around 1.4×10^{12} cm^{-2}. This is in the same order as that in a typical SiO_2 [18], and there is no obvious increase of AHT in Hf stacks, in contrast with the orders of magnitude increase of the as-grown electron traps in Hf stacks [5], [35]. The AHT does not appear being correlated with the as-grown electron traps for Hf stacks.

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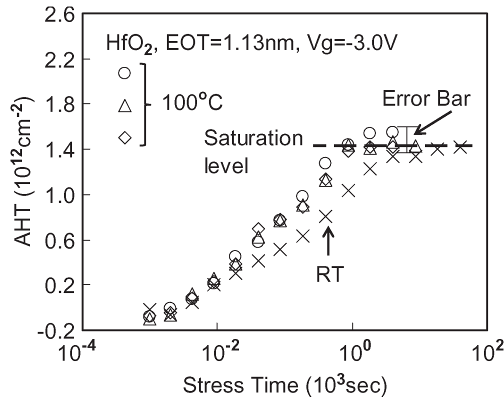

Fig. 9. Dependence of AHT on stress time and temperature. AHT is initially negligible but saturates at a level insensitive to the temperature. The test at 100 °C was repeated on three different devices to give the error bar.

E. Defect for the Loop-Shift

The loop-shift is not neutralized even when Vg is ramped to +1 V. Fig. 5 shows that ANPC has this property. In addition, it is well known that interface states can be created during stress. We will consider the generated interface states first and then ANPC.

1) Generated interface states ΔDit: For SiON, it has been suggested that ΔDit can dominate NBTI [36]. To find its contribution to the loop-shift of Hf stacks, Fig. 8 compares ΔDit with the total effective density of positive charges formed under negative bias stress ΔNth. Although ΔDit is negligible at short time (< 1 s), where the loop dominates, it becomes considerable as the stress time increases. However, the instability is not dominated by ΔDit for Hf stacks. ΔDit eventually saturates around 1.3×10^{12} cm^{-2} eV^{-1}, broadly agreeing with the well-known inherent density of P_{b0} centers [37] and the stress-induced saturation level for SiO_2/Si interface states [38]. This confirms that the recovery of generated interface states is insignificant in our case. As a result, ΔDit cannot be responsible for the up-loop, which is recoverable.
2) ANPC: The ANPC is the positive charge that can survive neutralization even under $Vg > 0$. We will show that it is the only defect responsible for two features of ΔVth, i.e., a reduction for higher measurement temperature and nonsaturation against stress time.

To examine the effect of measurement, rather than stress, temperature on ΔVth, the number of defects should be fixed when varying the measurement temperature. This can be achieved by first annealing a device at the highest measurement temperature (200 °C) for 30 min after stress, during which the initial rapid recovery occurred and the defect density was stabilized [29]. The device was then cooled down to room temperature (25 °C), and the measurement temperature varies in the following sequence:

$$25\,^\circ\mathrm{C} \rightarrow 65\,^\circ\mathrm{C} \rightarrow 100\,^\circ\mathrm{C} \rightarrow 150\,^\circ\mathrm{C} \rightarrow 200\,^\circ\mathrm{C}.$$

Fig. 10(a) clearly shows that, for a given number of defects, ΔVth actually progressively reduces as the measurement temperature increases. To confirm that the number of defects

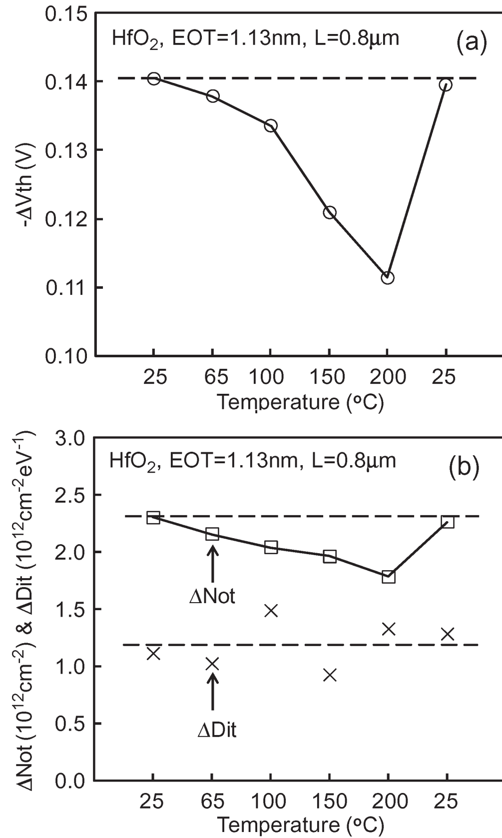

Fig. 10. Dependence of the instability on the measurement temperature. A device was first stressed at $Vg = -2.5$ V for 17 h at 25 °C. It was then annealed at 200 °C for 30 min with gate floating, during which the initial rapid recovery occurred. After stabilization of the defect, the measurement temperature was varied. (a) ΔVth reduces for higher measurement temperature for a given number of defects. (b) The positive charge density ΔNot behaves like ΔVth, but ΔDit is insensitive to measurement temperature.

remain the same during the above temperature sequence, the device was cooled down to 25 °C again after measuring at 200 °C. Fig. 10(a) shows that the ΔVth measured at 25 °C at the start and end of the above sequence agrees well, so the defect density changed little during the above measurement sequence.

To find out the origin of this measurement temperature dependence of ΔVth, Fig. 10(b) shows the dependence of ΔNot and ΔDit on the measurement temperature. ΔDit is insensitive to temperature, whereas ΔNot behaves similar to ΔVth. As a result, the dependence of ΔVth on the measurement temperature originates from the positive charge in Hf stacks.

To show this temperature dependence coming from ANPC, Fig. 11 presents the ANPC measured at different temperatures. It is clear that ANPC is enhanced as the temperature reduces from 150 °C to 25 °C, but CPC remains the same. As shown in Fig. 9, AHT is not responsible for this temperature dependence of ΔVth. Fig. 4(b) illustrates that the energy level of ANPC is above the bottom edge of the silicon conduction band. An increase of temperature enhances the number of electrons that can reach the ANPC and, consequently, reduces the positive charge. This sensitivity to measurement temperature implies that the antineutralization feature of ANPC cannot be explained by assuming it being located further away from the dielectric/substrate interface [9], [10], since tunneling is not sensitive to temperature.

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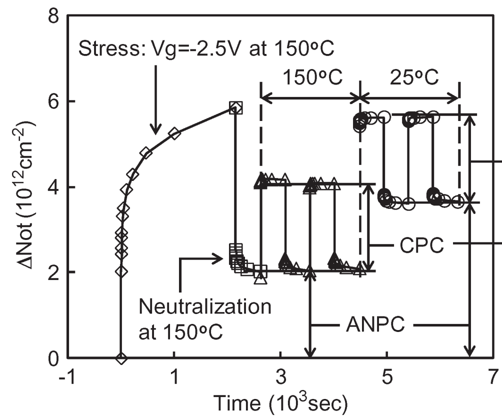

Fig. 11. Dependence of different types of positive charge on measurement temperature. The initial test sequence is the same as that in Fig. 5(a). After measurement at the stress temperature of 150 °C, the device was cooled down to 25 °C, and both CPC and ANPC were assessed again. It is clear that ANPC increases for lower measurement temperature, but CPC does not.

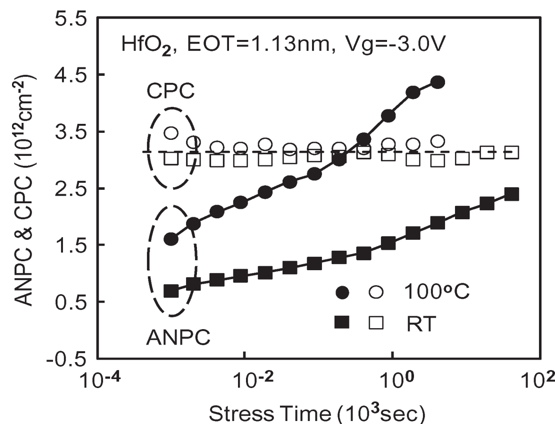

Fig. 12. Dependence of ANPC and CPC on stress time and temperature. ANPC increases with both stress temperature and time, but CPC does not.

Fig. 8 shows that a positive charge built up without saturation as the stress time increases, although the interface states saturate. Fig. 9 shows that AHT also saturates. Fig. 12 shows that the generated ANPC is the only defect responsible for the non-saturation of threshold voltage instability against stress time.

V. Conclusion

In this paper, the impact of positive charging on the performance of pMOSFETs has been studied. Three components of threshold voltage instability are unambiguously identified, i.e., loop, loop-shift, and up-loop. When a pulse is applied to the gate, the TCs measured at the second edge of the pulse do not follow that at the first edge, leading to the formation of a loop. It dominates the Vth instability at relatively short time (< 1 s). For longer time, the whole loop is shifted in the negative direction, although the loop size changes little. Unlike the loop, the up-loop cannot readily be recharged after neutralization.

A framework has been proposed for the defect, and the relation between each type of defect and Vth instability is clarified. In addition to the generated interface states, three kinds of positive charge exist in Hf stacks, i.e., CPC, ANPC, and AHT. Each type of defect has its unique signatures and can unambiguously be separated from the rest. CPC can repeatedly be charged and discharged by alternating the gate bias polarity. It is insensitive to measurement temperature and stress time, and is responsible for the loop. AHT is responsible for the up-loop, which is readily neutralized but not recharged at short stress time. As the stress time increases, it saturates. The loop-shift originates from both generated interface states and ANPC. ANPC is more difficult to neutralize than CPC and AHT, and is generated by the stress. It is the only defect that does not saturate with stress time and is responsible for the observed dependence of ΔVth on the measurement temperature. This framework for positive charges is not process specific, although the magnitude of positive charges depends on the process condition.

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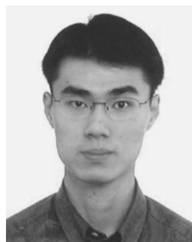

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