# Energy and Spatial Distributions of Electron Traps Throughout $SiO_2/Al_2O_3$ Stacks as the IPD in Flash Memory Application

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***Abstract*—$SiO_2$/high-$\kappa$ dielectric stacks will soon replace the conventional $SiO_2$-based dielectric stacks in Flash memory cells, as the thickness of $SiO_2$-based stacks is approaching its fundamental limit. The electron trap density in high-$\kappa$ layers is orders of magnitude higher than that in $SiO_2$, which may introduce excessive leakage via trap-assisted tunneling current and become the limiting factor for the retention of memory cells. Understanding the properties of electron traps throughout the dielectric stack is essential for estimating the leakage current and for selecting materials and processes in order to reduce the leakage. However, detailed information on trap properties in the bulk of high-$\kappa$ layers is still missing. A recently developed two-pulse $C$–$V$ measurement technique is used in this paper to investigate the energy and spatial distribution of electron traps throughout the $SiO_2/Al_2O_3$ dielectric stacks. Four energy regions of electron traps have been observed. The shallower traps mainly above the Si conduction band bottom $E_{CB}$ are found distributed across the $Al_2O_3$ layer. A narrow band of traps below Si $E_{CB}$ with a bandwidth of about 0.1 eV can be observed near the $SiO_2/Al_2O_3$ interface. Traps in the midlevel region corresponding to Si bandgap and traps in the deeper energy region mainly below Si valence band top are also observed. The postdeposition annealing in $N_2$ has different impacts on the electron traps in different energy regions.**

***Index Terms*—$Al_2O_3$, electron trap, energy distribution, Flash memory, floating gate, high-$\kappa$ dielectrics, interpoly dielectric (IPD) layer, pulsed $C$–$V$.**

## I. Introduction

THE RAPID growth of the Flash memory market has been driven by the increase of memory capacity and the decrease of unit price, due to the continuous downscaling of Flash memory cells [1]–[4]. However, the scaling of the conventional $SiO_2$-based tunnel and control dielectric layers in Flash memory technology is fast approaching its limits [2], as increasing leakage current through thinner $SiO_2$ layers will result in a fast data loss [3]. According to the ITRS Roadmap 2007 [4], this becomes the most pressing issue to be solved for floating-gate Flash memory. Furthermore, starting from the 45–40-nm technology generation for floating-gate Flash devices, the spacing between two adjacent floating gates becomes too small to allow the control gate to overlap the floating gate on the vertical sidewalls in minimum feature-sized cells [2], [3]. In order to maintain the coupling ratio, this will require a further reduction of the dielectric thickness between control and floating gates, i.e., the interpoly dielectric (IPD), which will, in turn, inevitably increase the leakage and degrade the data retention.

The introduction of high-$\kappa$ materials as the IPD in floating-gate Flash memory has been proposed as a potential solution [2]–[6]. Higher dielectric constant will increase the IPD capacitance without reducing its physical thickness and therefore help in maintaining the coupling ratio and allow the cell size to continue downscaling. A large amount of work has been carried out to investigate the capabilities and limits of using high-$\kappa$ layers to replace the conventional oxide–nitride–oxide stack by a number of research groups [6]–[12], in order to reduce the equivalent thickness of IPD from $\sim$15 nm to less than 10 nm. The key issues are the capabilities of the $SiO_2$/high-$\kappa$ layers to provide enough program/erase windows, sufficient data retention and endurance, and most importantly, a low leakage to guarantee the ten-year retention.

It has been reported that the density of electron traps in high-$\kappa$ layers is orders of magnitude higher than that in conventional $SiO_2$ [13]–[15], which may induce excessive low-field leakage current through trap-assisted tunneling [16]. Understanding the properties of electron traps throughout the dielectric stack is essential not only for estimating the low-field leakage current responsible for data retention but also for selecting materials and process conditions to suppress the leakage. However, detailed information on trap properties in the bulk of high-$\kappa$ layers, particularly on their energy and spatial distributions, is still missing. It has also been reported that postdeposition annealing (PDA) at different temperatures significantly changes the microstructure of high-$\kappa$ layers, which may, in turn, affect the properties of electron traps [17]. This offers a way for reducing electron traps in the high-$\kappa$ layer through optimizing PDA temperature. There is, however, little quantitative information on how PDA affects electron traps, particularly in terms of their energy and spatial distributions.

Several groups have recently used various charge-pumping (CP) methods to probe the trap distribution in high-$\kappa$ layers

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[18]–[22]. It has been reported that, with a 1-nm interfacial layer, the deepest traps that CP can probe are about 1 nm into the high-$\kappa$ layer, when the frequency drops to 100 Hz, below which the CP current is too small to measure [21]. The target high-$\kappa$ layer to be used in the floating-gate Flash memory cells are much thicker, usually in the range of 5–15 nm, so that majority of the film is beyond the reach of even advanced CP techniques. The interfacial $SiO_2$ layer in Flash memory cells may also be thicker than 1 nm [2], [3], which, in turn, reduces the depth in the high-$\kappa$ layer that can be probed by CP measurements.

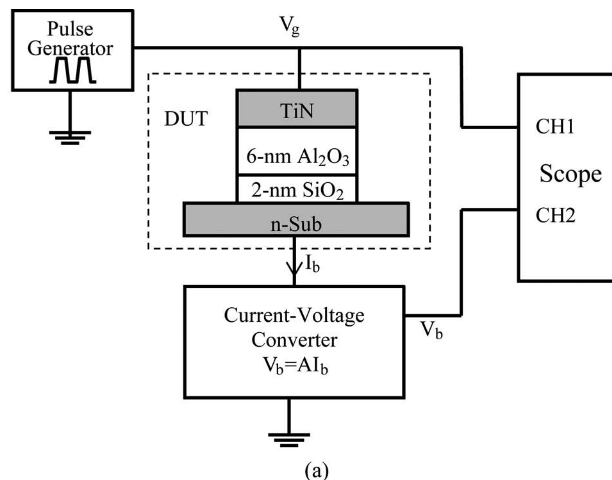
Other existing techniques commonly used for dielectric characterization include capacitance–voltage ($C$–$V$) [9], conductance [23], transfer characteristics ($I$–$V$) [24], and pulsed $I$–$V$ measurements [14], [24], [25]. The traditional $C$–$V/I$–$V$ measurements have been used to probe charge loss at long timescales [26], [27], and photo-$I$–$V$ technique was used to assess the spatial distribution of charges [28], but these measurements are too slow to characterize the defects near the interface because of fast detrapping [24], [27]. To improve the measurement speed, the single pulse $I$–$V$ technique was developed, but it did not give the energy and spatial distribution of defects [24], [25].

We have recently developed a two-pulse $C$–$V$ measurement technique that can overcome the shortcomings of conventional techniques and probe the electron traps throughout the $SiO_2$/high-$\kappa$ stack [29]. It was shown that electron traps in the bulk of the high-$\kappa$ layer indeed dominate the trapping [29]. In this paper, electron trap energy and spatial distributions throughout the $SiO_2/Al_2O_3$ stack are investigated by using the two-pulse $C$–$V$ technique, and the impact of PDA temperature on electron trap distributions is also studied. This paper is organized as follows. After a description of the devices and measurement technique in Section II, the methodology used to define the dischargeable energy levels of electron traps across the dielectric stack is given in Section III-A. The energy and spatial distributions of electron traps are reported in Sections III-B and C, respectively.

## II. Devices and Experiments

### A. Devices

$SiO_2/Al_2O_3$ MOS capacitors were fabricated at IMEC using a process flow similar to that used for forming the IPD stacks in floating-gate Flash memory devices. A 2-nm-thick high-temperature oxide was deposited as the bottom layer on an n-type Si substrate without p-n junctions. A 6-nm $Al_2O_3$ layer was then prepared by atomic layer chemical vapor deposition. The $SiO_2/Al_2O_3$ stack has an EOT of about 4.6 nm. The deposition was followed by a conventional postdeposition anneal for 60 s in $N_2$ at 800, 900, or 1000 °C. Device fabrication was completed by deposition and etching of a TiN gate. $Al_2O_3$ dielectric constant $\varepsilon_{\mathrm{Al2O3}} = 9.3$ were determined from high-frequency CV measurements. The capacitor size is $9 \times 10^{-4}$ cm$^2$. The effects of $Al_2O_3$ thickness contraction at high PDA temperature have been taken into account in the analysis [22].



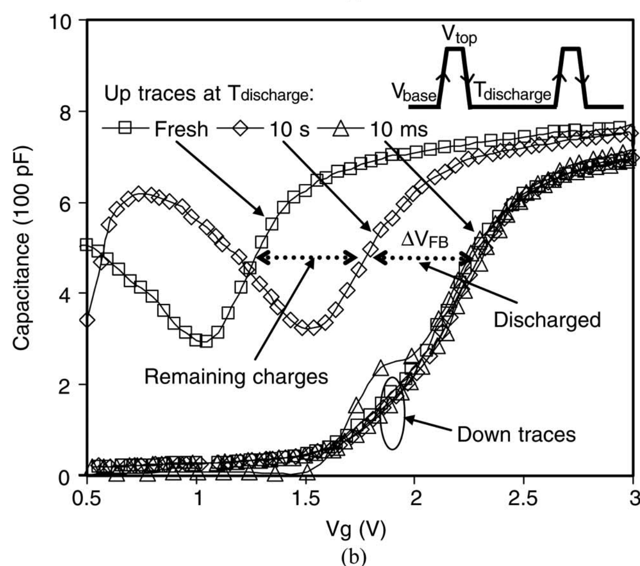




Fig. 1. (a) Simplified diagram of the pulsed $C$–$V$ test setup, where $I_b$ is the bulk current and $V_b$ is the output of the current–voltage converter. $V_g$ is the output of the pulse generator. Both $V_g$ and $V_b$ are recorded by an oscilloscope. (b) Inset shows the $V_g$ waveform in a typical two-pulse $C$–$V$ test. The first pulse is used to charge the capacitor. The flatband voltage determined from the first ramp-up trace on a fresh device is the fresh $V_{\mathrm{FB}}$ value without charge trapping, and the flatband voltage after electron trapping can be determined from the ramp-down trace. The capacitor is then discharged for a period of time $T_{\mathrm{discharge}}$ under a gate bias of $V_{\mathrm{base}}$ until the beginning of the second pulse. The amount of discharge can be determined by the flatband voltage shift between the ramp-up trace of the second pulse and the first ramp-down trace $\Delta V_{\mathrm{FB}}$. Typical test conditions used in this paper are as follows. The top voltage level of the pulse is 5 V, and the pulsewidth is 1 ms, to emulate the voltage drop across the IPD layer in floating-gate memory cells during a typical programming session. The base voltage level $V_{\mathrm{base}}$ is varied between $-3$ V and the flatband voltage. The ramp-up/ramp-down rate on the rising/falling edges is set to a high level of 10 kV/s to minimize the charging/discharging during the CV measurement.

### B. Experiments

The pulsed $C$–$V$ technique [30]–[32] is used to measure the flatband voltage, and a simplified setup diagram is shown in Fig. 1(a). The system consists of a Keithley 428 current amplifier, an Agilent 81110A pulse generator, and a Tektronix TDS460A oscilloscope. All instruments are controlled by a computer. A two-pulse $C$–$V$ technique was further developed to measure the flatband voltage shift caused by charging and

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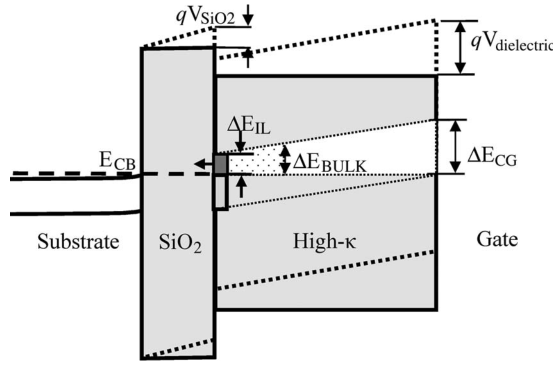


Fig. 2. Energy band diagram of the $SiO_2/Al_2O_3$ stack during discharge. $\Delta E_{\rm IL} = qV_{\rm SiO2}$ is the increased energy level of electron traps at the $SiO_2$/high-$\kappa$ interface, and $\Delta E_{\rm CG} = qV_{\rm dielectric}$ is the trap energy level increased at the control gate interface, where $V_{\rm SiO2}$ and $V_{\rm dielectric}$ are the potential drops across the $SiO_2$ and $SiO_2$/high-$\kappa$ stack, respectively. $\Delta E_{\rm BULK}$ is the increased energy level of electron traps inside the bulk of the high-$\kappa$ layer, which increases with the distance to the $SiO_2/Al_2O_3$ interface.

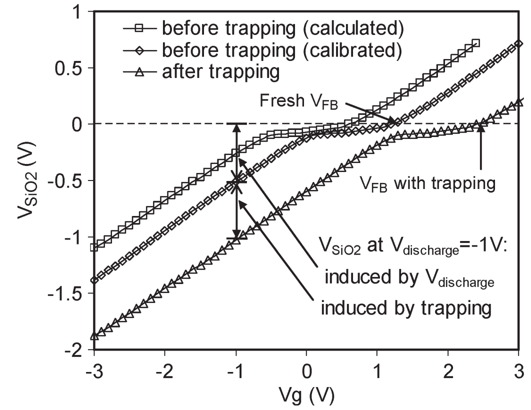


Fig. 3. Relation between $V_{\rm SiO2}$ and gate bias $V_g$ calculated using (1). The symbol "□" represents the calculated results assuming ideal dielectric layers without electron trapping. The symbol "◇" represents the calibrated results on a fresh device after taking into account the as-grown fixed charge in the $Al_2O_3$ layer. Calibration was achieved by shifting the ideal $V_{\rm SiO2}-V_g$ curve toward the positive direction along the $V_g$ axis so that the $V_{\rm FB}$ agrees with the measurement. Symbol "Δ" represents the relation between $V_{\rm SiO2}$ and $V_g$ when there exists electron trapping. To take into account the effects of different trapping levels, the $V_{\rm SiO2}-V_g$ curve was shifted along the $V_g$ axis so that $V_{\rm FB}$ equals to the measured value at each measurement step during the charging/discharging. $V_{\rm SiO2}$ was then obtained from the shifted curve at the corresponding $V_{\rm charge}/V_{\rm discharge}$.

discharging the traps in the dielectric stack [29]. The waveform of the two gate pulses is shown in the inset of Fig. 1(b). The first pulse is used to charge the capacitor, and the flatband voltage after electron trapping can be determined from its ramp-down trace. The capacitor is then discharged for a period of time $T_{\rm discharge}$ under a gate bias of $V_{\rm base}$ until the beginning of the second pulse. The amount of discharge can be determined by the flatband voltage shift between the ramp-up trace of the second pulse and the ramp-down trace of the first pulse.

Fig. 1(b) shows a typical measurement result with variable $T_{\rm discharge}$ at $V_{\rm base} = -1$ V. The difference between the up and down traces of the first pulse on a fresh device gives the total amount of trapping. The up trace of the second pulse overlaps with the down traces at a short discharge time such as 10 ms and then moves toward the left when $T_{\rm discharge}$ increases, indicating an increase of discharge. $V_{\rm FB}$ does not return to its fresh value after 10 s of discharge, indicating that some electrons are still trapped in the high-$\kappa$ layer. The $V_{\rm FB}$ difference between the up and down traces $\Delta V_{\rm FB}$ is used as the measure of the discharged trap density. Since there is no limit on the maximum $T_{\rm discharge}$, this provides an effective way to overcome the shortcomings of CP techniques and to probe defects across the $SiO_2$/high-$\kappa$ stack [29].

## III. Results and Discussions

### A. Dischargeable Trap Energy Levels Across the $SiO_2/Al_2O_3$ Stack

It has been reported that the energy distribution of electron traps at the $SiO_2$/high-$\kappa$ interface can be measured by CP with variable base levels [19]. As shown in Fig. 2, only electron traps with an energy level higher than the silicon conduction band bottom can be discharged via tunneling, since there are little empty states in the silicon band gap. If the gate bias is increased to $V_g$, the potential drop across the $SiO_2$ layer will increase accordingly to $V_{\rm SiO2}$. The energy level of electron traps in the high-$\kappa$ layer at the $SiO_2$/high-$\kappa$ interface will also increase by $\Delta E_{\rm IL} = qV_{\rm SiO2}$. For fresh samples without trapping, $\Delta E_{\rm IL}$ and $qV_{\rm SiO2}$ can be estimated as [22]

$$\Delta E_{\rm IL} = qV_{\rm SiO2} = q\frac{(V_g - V_{\rm FB} - \Phi_S)}{1 + \frac{\varepsilon_{\rm SiO2}}{\varepsilon_{\rm Al2O3}}\frac{t_{\rm Al2O3}}{t_{\rm SiO2}}} \quad (1)$$

where the flatband voltage $V_{\rm FB}$ and surface potential $\Phi_S$ can be calculated using the model described in [33]. The energy spectroscopy of electron traps near the $SiO_2$/high-$\kappa$ interface can be measured by sweeping the discharge bias and measuring the amount of discharge at the corresponding energy level $\Delta E_{\rm IL}$. For example, at a negative bias, the potential across the $SiO_2$ layer increases. Traps at energy levels corresponding to the white region in the high-$\kappa$ layer in Fig. 2 become dischargeable as their energy levels are increased to above the Si $E_{\rm CB}$. Deeper traps in the shadowed region remain charged as there are little empty states in Si band gap. By increasing $V_{\rm base}$ sequentially and measuring the complete discharge between two successive $V_{\rm base}$'s, trap density against energy level can be measured.

The $V_{\rm SiO2}$ against gate bias $V_g$ for a 2-/6-nm $SiO_2/Al_2O_3$ stack is calculated using (1), and the results are shown in Fig. 3. It was observed that the measured flatband voltage of a fresh device was 0.6 V higher than the calculated value. This can be attributed to the existence of fixed as-grown negative charges in the $Al_2O_3$ layer [34]. To correct the effects of these charges, the calculated $V_{\rm SiO2}-V_g$ curve was calibrated by shifting toward the positive direction along the $V_g$ axis so that its $V_{\rm FB}$ agrees with the measurements, and the calibrated results are used as the $V_{\rm SiO2}-V_g$ curve.

During the charging/discharging, the electron trapping level changes significantly due to the high trap density in $Al_2O_3$. This causes $V_{\rm FB}$ to shift accordingly and, in turn, changes the $V_{\rm SiO2}-V_g$ curve. To take into account the effects of trapping level on the potential drop across the $SiO_2$ layer, the $V_{\rm FB}$

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measured at each charging/discharging step is used as the monitor of the effective trapping level in the dielectric stack, and the $V_{SiO2}-V_g$ curve was shifted along the $V_g$ axis so that $V_{FB}$ equals the measured value. $V_{SiO2}$ and, therefore, $\Delta E_{IL}$ at the $SiO_2$/high-$\kappa$ interface were then obtained from the shifted curve at the corresponding gate bias, as shown in Fig. 3. The total $V_{SiO2}$ consists of two components: One is induced by the gate bias, for example, $V_{discharge} = -1$ V during discharging, and the other one is induced by the trapping, i.e., $\Delta V_{FB}$ measured at the corresponding discharging step. This first-order correction is more accurate at larger gate biases. Here, it is assumed that the trapping in the $SiO_2$ interfacial layer and trapping/detrapping during the CV measurement are small and negligible, as shown in [29]. It is also assumed that the detrapping is dominated by tunneling, and the effect of thermal detrapping associated with lattice energy is negligible.

When moving farther into the bulk of the high-$\kappa$ layer, the energy levels of electron traps will be further elevated due to the potential drop across the high-$\kappa$ layer, as shown in Fig. 2. $\Delta E_{CG}$, the trap energy level that is changed at the control gate interface, can be obtained as

$$\Delta E_{CG} = qV_{dielectric} = q(V_g - V_{FB} - \Phi_S) \qquad (2)$$

where $V_{dielectric}$ is the potential drop across the $SiO_2$/high-$\kappa$ stack. The energy levels elevated inside the bulk of the high-$\kappa$ layer $\Delta E_{BULK}$ vary between $\Delta E_{IL}$ and $\Delta E_{CG}$. $\Delta E_{BULK}$ increases with the distance from the $SiO_2$/high-$\kappa$ interface, indicating that deeper traps become dischargeable when moving farther away from the interface. Therefore, the spatial location should also be taken into consideration when analyzing the energy distribution of traps in the bulk of the high-$\kappa$ layer. Based on the aforementioned analysis, the energy and spatial distribution of electron traps throughout the $SiO_2/Al_2O_3$ stack are assessed in the following sections.

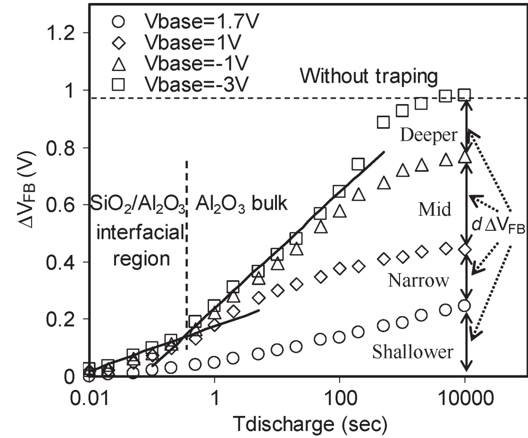


Fig. 4. Discharge-induced $\Delta V_{FB}$ against discharge time at various $V_{base}$. The test conditions are the same as that in Fig. 1. The dashed horizontal line is the total trapping level. The two solid lines are linear fittings to the data at $V_{base} = -3$ V before and after the slope changes. Their intersection at 200 ms indicates the transition time from $SiO_2$ to $Al_2O_3$.

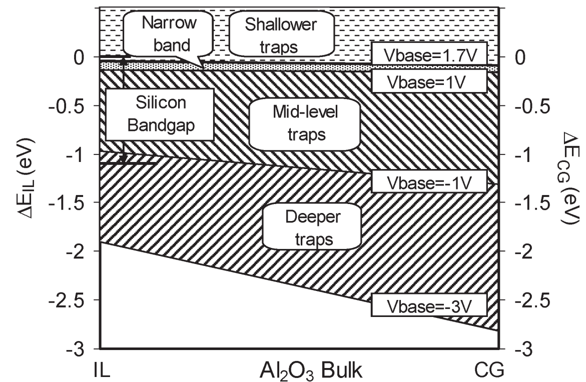


Fig. 5. Illustration of dischargeable energy regions with respect to the Si $E_{CB}$ at the corresponding discharge bias. For a given $V_{base}$, $\Delta E_{IL}$ and $\Delta E_{CG}$ are calculated using (1) and (2), respectively, as described in Section III-A. A straight line is used as the boundary between two adjacent regions, as a first-order approximation.

### *B. Energy Distribution of Electron Traps*

In order to investigate trap distributions across the dielectric stack, discharge is carried out at several biases, and $\Delta V_{FB}$ is shown against discharge time in Fig. 4. The change in the slope of $\Delta V_{FB}$ versus $\log(T_{discharge})$ at about 200 ms when moving into the high-$\kappa$ layer confirms that trapping density in $Al_2O_3$ is higher than that in $SiO_2$, and trapping is dominated by $Al_2O_3$. The excellent agreement between the discharge saturation after approximately 1000 s at $V_{base} = -3$ V and the total trapping level confirm that 100% discharge was achieved. This demonstrates the capability of the two-pulse $C$–$V$ technique for probing traps throughout the entire stack.

As shown in Fig. 2, when the gate bias increases in absolute value, the energy level of electron traps at the $SiO_2$/high-$\kappa$ and gate interfaces will increase by $\Delta E_{IL} = qV_{SiO2}$ and $\Delta E_{CG} = qV_{dielectric}$, respectively, and traps within this energy region become dischargeable. The discharge biases $V_{base}$ used in Fig. 4 are carefully selected by using (1) so that electrons discharged from four energy regions in the $Al_2O_3$ bandgap can be studied, as shown in Fig. 5: the shallower region mainly above Si $E_{CB}$, the narrow region near Si $E_{CB}$ with a bandwidth of about 0.1 eV, the midlevel region mainly corresponding to Si bandgap, and the deeper region mainly below Si valence band top. For a given $V_{base}$, $\Delta E_{IL}$ and $\Delta E_{CG}$ are calculated using (1) and (2), as described in Section III-A. The differences in $\Delta V_{FB}$ at different $V_{base}$'s in Fig. 4, i.e., $d\Delta V_{FB}$, are caused by discharging traps within the corresponding region.

Fig. 6(a) shows the comparison of the total trapping density in each energy region for three samples with different PDA temperatures. Trapping in all regions are within the same order of magnitude, with the highest trapping observed in the midlevel region corresponding to Si bandgap and the lowest trapping in the narrow region near Si $E_{CB}$. It should also be noted that, although $d\Delta V_{FB}$ is the lowest for the narrow region, the trap density per electronvolt is actually the highest here due to its small bandwidth of about 0.1 eV, which results in the trap density per electronvolt nearly one order of magnitude higher than other regions, as shown in Fig. 6(b). It is also possible that this narrow region can be regarded as a discrete trap level.

Fig. 6(a) and (b) clearly shows that PDA temperature has significant impact on trapping density in different

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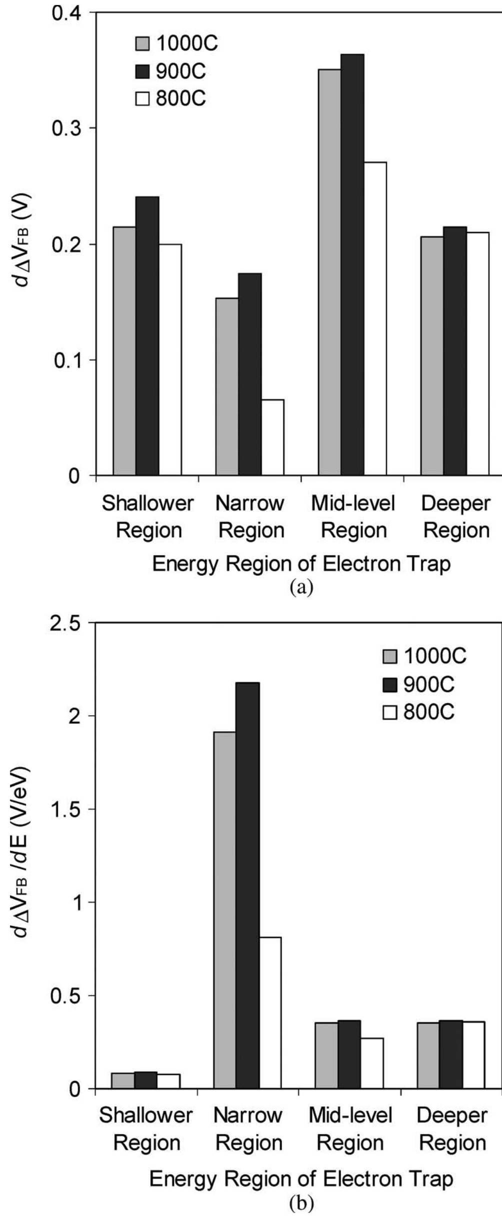


Fig. 6. (a) Total trapping in each energy region for three samples with PDA in $N_2$ at 800 °C, 900 °C, and 1000 °C, respectively. (b) Trapping densities per electronvolt in each region.

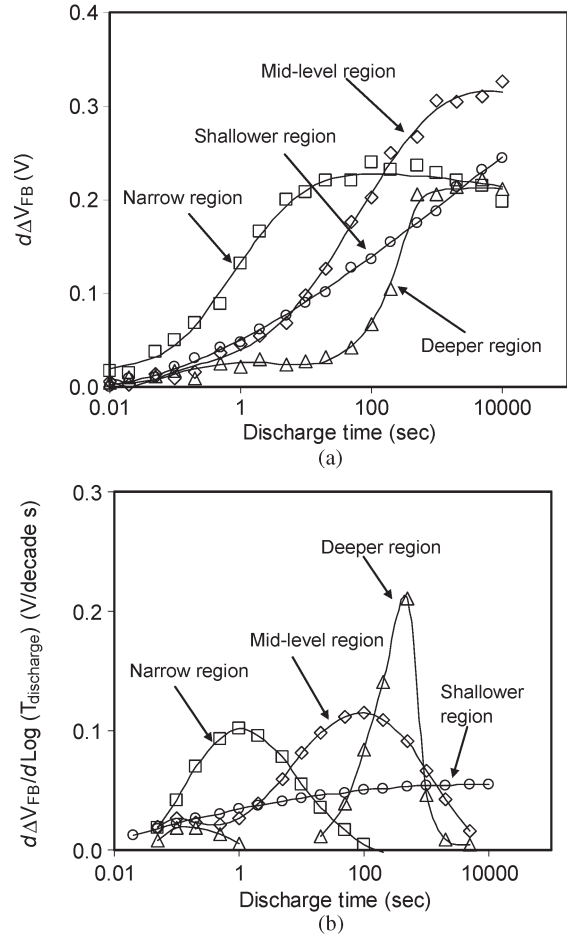


Fig. 7. (a) Discharge against $T_{\mathrm{discharge}}$ in each region for the sample with PDA in $N_2$ at 900 °C. The symbols are the experimental data, and the solid lines are smoothed fittings. (b) Discharge rate against $T_{\mathrm{discharge}}$ obtained from the derivative of $\Delta V_{\mathrm{FB}}$ against $T_{\mathrm{discharge}}$ by using the fittings in Fig. 7(a).

energy regions. While the difference in trapping is insignificant in all regions when PDA temperature reduces from 1000 °C to 900 °C, a further decrease of temperature to 800 °C, however, leads to a clear decrease of trapping. This is in agreement with the observation that $Al_2O_3$ is crystallized at temperatures above 800 °C and that crystallization may introduce additional electron traps [17]. The largest reduction occurs in the narrow region near $E_{\mathrm{CB}}$. The reduction is 67%, 27%, 17%, and 2% in the narrow, mid, shallower, and deeper regions, respectively. As a result, the PDA temperature mainly affects electron traps near $E_{\mathrm{CB}}$ and in the Si bandgap, where the O-vacancy is located [35]. It should be noted that, despite the increased trap density, better retention has been observed in memory cells with crystallized $Al_2O_3$ IPD layers [16]. This is attributed to its increased $SiO_2/Al_2O_3$ band offset from 2.3 to 2.6 eV [16], [22], which compensates for the increase in the trap density, therefore reducing the leakage.

### C. Spatial Distribution of Electron Traps

Given a long-enough discharge time, electron traps throughout the $Al_2O_3$ layer can be discharged, as shown in Fig. 4. To assess their spatial location, Fig. 7(a) shows the discharge against time in each energy region. Since the electron tunneling time increases exponentially with tunneling distance, the tunneling depth is a linear function of $\log(T_{\mathrm{discharge}})$ [18], [26]. Within a given distance range, higher trap density will result in a higher amount of discharge for the same increase in $\log(T_{\mathrm{discharge}})$. A longer time corresponds to discharge farther away from the substrate. For traps within the narrow region near $E_{\mathrm{CB}}$, the increase only occurs between 200 ms and 10 s, indicating that these traps are close to the $SiO_2/Al_2O_3$ interface, mainly located in the transition region between $SiO_2$ and $Al_2O_3$. Similar results have also been observed by using CP techniques, where electron traps are observed at energy levels just below the Si conduction band bottom at the interface of $SiO_2/Al_2O_3$ [22]. This is not surprising as the interfacial region is a transition between two types of materials, and it is expected that the microstructure at the interface is different from that

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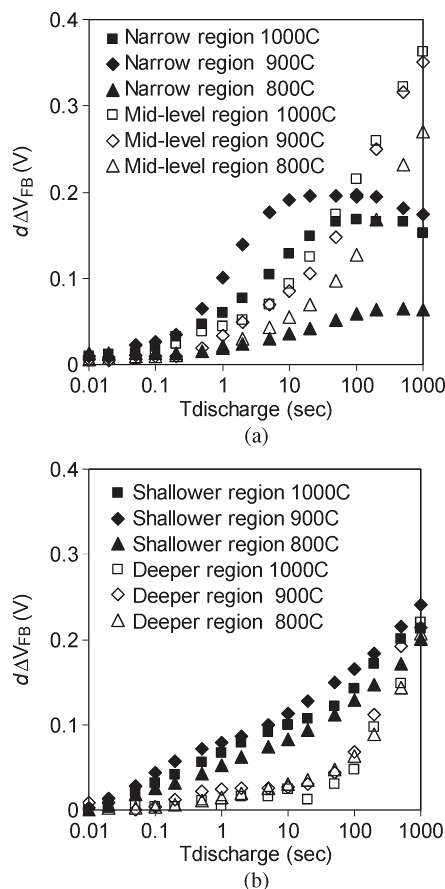


Fig. 8. Discharge against $T_{\text{discharge}}$ in each region for three samples with PDA in $N_2$ at 800 °C, 900 °C, and 1000 °C, respectively. Fig. 8(a) shows the narrow and midlevel regions. Fig. 8(b) shows the shallower and deeper regions.

in the bulk. Since these traps are located within the transition region only, their density can be used as an indicator of the interface quality between $SiO_2$ and $Al_2O_3$.

For traps in the midlevel region, the increase starts after several seconds, and for the deeper region, the increase of slope starts from 100 s. This can be clearly seen in Fig. 7(b), where the slopes for each energy region are compared. There is a peak for traps in the narrower, mid, and deeper regions, respectively, indicating that traps are not uniformly distributed in $Al_2O_3$. Traps within the deeper energy region are situated near the gate interface, and traps within the midlevel region are mainly in the $Al_2O_3$ bulk. There is no apparent peak for the shallower traps, suggesting that they are distributed across the $Al_2O_3$ layer.

The comparison of the impact of PDA temperature on trap spatial location is shown in Fig. 8(a) and (b). In comparison with the 800 °C result, there is a sharp rise in the narrow region after 900 °C PDA, indicating that the traps near $E_{\text{CB}}$ are mainly generated by high PDA temperatures, suggesting a crystallization-related type of defect. The rise occurs mainly between $T_{\text{discharge}} = 1$ and 10 s, corresponding to the transition region between $SiO_2$ and $Al_2O_3$. In contrast, higher PDA temperatures only induce a modest increase of trapping in the shallower and midlevel regions and no increase in the deeper region. There is no significant change in the slopes for these three regions, indicating that PDA has little effects on the location of these traps.

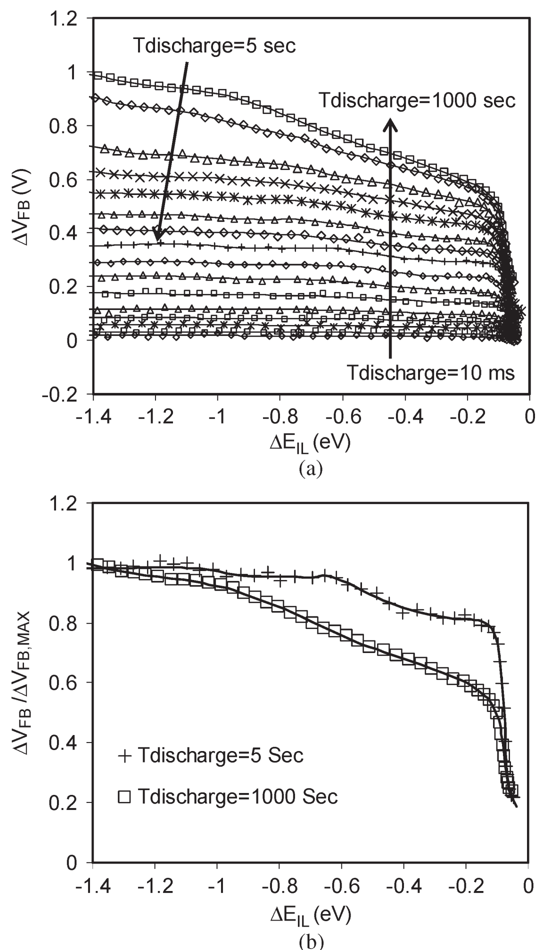


Fig. 9. (a) $\Delta V_{\text{FB}}$ caused by discharge at different $\Delta E_{\text{IL}}$ and $T_{\text{discharge}}$ for the sample with PDA in $N_2$ at 900 °C. Test conditions are the same as in Fig. 1. The symbols denote the experimental data, and the solid lines represent the smoothed polynomial fittings. Each data point is obtained by a two-pulse measurement during the discharge, and its corresponding $\Delta E_{\text{IL}}$ is obtained from the $V_{\text{base}}$ and the measured $\Delta V_{\text{FB}}$, as shown in Fig. 3. (b) Curves at $T_{\text{discharge}}$ of 5 and 1000 s in Fig. 9(a) are compared after being normalized by their maximum $\Delta V_{\text{FB}}$.

Further experiments on the samples with PDA at 900 °C are also carried out to investigate the discharging behavior against $\Delta E_{\text{IL}}$ at various discharge times. The results are shown in Fig. 9(a), where each data point is obtained by a two-pulse measurement during the discharge and its corresponding $\Delta E_{\text{IL}}$ is obtained from the $V_{\text{base}}$ and the measured $\Delta V_{\text{FB}}$, as shown in Fig. 3. Several features can be observed:

1) $\Delta V_{\text{FB}}$ at a constant $\Delta E_{\text{IL}}$ increases with discharge time. Since longer discharge time allows traps located farther away from the substrate to be discharged [17], [26], this increase is caused by the discharge of traps farther in the bulk of the $Al_2O_3$ layer.
2) For traps deeper than $\Delta E_{\text{IL}} = -0.8$ eV, $\Delta V_{\text{FB}}$ increases with $\Delta E_{\text{IL}}$ at long discharge times, but changes little at short discharge times. This is clearly shown in Fig. 9(b), where the curves at $T_{\text{discharge}}$ of 5 and 1000 s are compared after being normalized by their maximum $\Delta V_{\text{FB}}$. It suggests that, at short discharge times, traps below $\Delta E_{\text{IL}} = -0.8$ eV discharge little, in agreement with the

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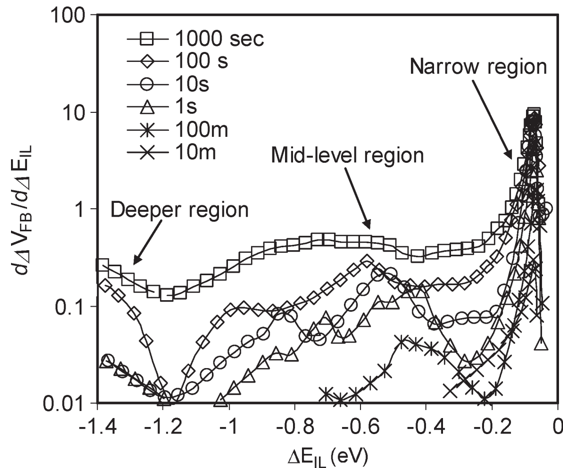


Fig. 10. Discharge rate against $\Delta E_{\rm IL}$ obtained from the derivative of $\Delta V_{\rm FB}$ in Fig. 9(a) by using the smoothed fittings. $d\Delta V_{\rm FB}/d\Delta E_{\rm IL}$ is shown on the logarithmic scale.

observation in Fig. 7(b), where deeper traps are farther away from IL interface and can be discharged within short $T_{\rm discharge}$.

3) Discharge increases sharply at $\Delta E_{\rm IL} \approx -0.1$ eV, indicating a high density of trapping at this energy level. This can be clearly seen in Fig. 10, in which the derivative of $\Delta V_{\rm FB}$ against $\Delta E_{\rm IL}$ is shown. It is worth noting that the derivative is obtained from the smoothed polynomial fittings (solid lines in Fig. 9) to reduce the noise [22]. It can be clearly observed that there is a large and a narrow peak at $\Delta E_{\rm IL} = -0.1$ eV caused by the sharp change of $\Delta V_{\rm FB}$, which agrees well with the narrow region observed in Fig. 6(b).
4) There are two other smaller and broader peaks in Fig. 10 when $\Delta E_{\rm IL}$ becomes deeper. These peaks are caused by the discharge of electron traps within the midlevel and deeper energy regions, which only become dischargeable at larger negative bias. This again supports the observation in Fig. 6(b).

It should be noted that $\Delta E_{\rm IL}$ is the trap energy level measured at the $SiO_2/Al_2O_3$ interface. As shown in Fig. 2, the energy level of dischargeable electron traps in the bulk of $Al_2O_3$ is deeper than that at the interface under the same bias. Therefore, a part of the traps measured at long discharge times should actually have deeper energy levels than the corresponding $\Delta E_{\rm IL}$. As shown in Fig. 10, the deeper peaks become broader with increased $T_{\rm discharge}$, and its position also moves toward deeper levels. It is also noted that Fig. 10 does not give the distribution for traps in the shallower region at $\Delta E_{\rm IL} \approx 0$ and above. This is because, in order to measure $V_{\rm FB}$ on the pulse edge, $V_{\rm base}$ must be smaller than $V_{\rm FB}$. Since $V_{\rm base}$ is the discharge bias and it cannot be swept above the flatband voltage, the information on the distribution of shallower traps cannot be obtained.

It is worth pointing out that only the relative spatial positions for traps within each energy region can be obtained here, as it is currently unknown whether electron trapping ends at the gate interface or in the bulk of $Al_2O_3$ layer. We cannot rule out the possibility that there might be a lack of trapping near the gate interface as traps close to the gate cannot be filled steadily due to tunneling to the gate or there might be a lack of traps near the gate because $Al_2O_3$ could be modified by interacting with the metal gate. The effects of electron trap energy levels on the extraction of trap spatial location have been considered only by dividing the energy into four regions, as shown in Fig. 2. Therefore, the spatial distribution is the average within each energy region. It is noted that the approach used in this paper is semiquantitative, in which possible concurrent trapping due to carrier injection from the gate is not accounted for, in order to simplify the interpretation of the results. Correlation of the discharge time with position inside the stack allows us to speculate that the traps within the deeper energy region are situated near the gate interface, while the traps within the midlevel region are mainly in the $Al_2O_3$ bulk. However, this needs to be validated by the numerical models, given that the present assumptions do not account for the gate-side injection nor have a quantitative time-to-space translation. Further work is underway to investigate the interplay between the trap energy levels and spatial locations, including developing a fully numerical model, which is beyond the scope of this paper and will be reported elsewhere. It is also worth noting that $\Delta V_{\rm FB}$ is used as the measure of trapping level in this paper. Trapping farther away from the IL interface contributes less to the flatband voltage shift, so that $\Delta V_{\rm FB}$ is less sensitive to it.

## IV. Conclusion

The energy regions and spatial locations of electron traps throughout $SiO_2/Al_2O_3$ dielectric stacks have been investigated in this paper by using the novel two-pulse $C$–$V$ technique, which allows the measurement of discharge behavior without the limitation of maximum discharge time.

Four energy regions of electron traps in the $Al_2O_3$ layer have been studied. It is found that shallower traps with energy levels mainly above the Si conduction band bottom are distributed across the $Al_2O_3$ layer, traps near Si conduction band bottom are located close to the $SiO_2/Al_2O_3$ interface, and traps in the midlevel region corresponding to Si bandgap and traps in the deeper energy region mainly below Si valence band top are also observed. The temperature of PDA in $N_2$ has a major impact on traps in the narrow region, a modest impact in the midlevel and shallower regions, and an insignificant impact in the deeper region. This shows that the discharge-based two-pulse technique can provide useful information on electron traps that is required for modeling the low-field leakage and retention in Flash memory cells.

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